2004

24GHz CMOS direct downconversion receiver front-end and VCO design

Jie Long
Iowa State University

NOTE TO USERS

2.4GHz CMOS direct downconversion receiver front-end and VCO design

by

Jie Long

A dissertation submitted to the graduate faculty

in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

Major: Electrical Engineering (Microelectronics)

Program of Study Committee:
Robert J. Weber, Major Professor
Eric Bartlett
Degang J. Chen
Julie A. Dickerson
Fritz Keinert

Iowa State University

Ames, Iowa

2004

Graduate College
Iowa State University

This is to certify that the doctoral dissertation of

Jie Long

has met the dissertation requirements of Iowa State University

Signature was redacted for privacy.

Major Professor

Signature was redacted for privacy.

For the Major Program

DEDICATION

I would like to dedicate this thesis to my wife Kai and to my daughter Mindy without whose support I would not have been able to complete this work. I would also like to thank my friends and family for their loving guidance and financial assistance during the writing of this work.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABSTRACT

The explosive growth of today's wireless communication market has brought an increasing demand for high performance radio-frequency (RF) circuits in low-cost technologies. Because of advancements in RF CMOS circuits, devices, and passive elements in the last decade, it has become possible to develop a RF system-on-chip (SoC) that integrates RF, analog and digital circuits completely. Direct downconversion, or zero-IF downconversion architecture, shows an advantage over traditional superheterodyne architectures, because it eliminates the image rejection filter and IF filter, and employs only one local oscillator (LO), which reduces the receiver size and power dissipation significantly. For this reason, direct downconversion has drawn more and more attention recently in various wireless applications. However, direct downconversion also presents some design challenges like flicker noise, DC offsets, even-order distortion, and I/Q mismatches. In this work, a thorough noise analysis and a comprehensive study of the noise mechanism of the low noise amplifier of CMOS direct downconversion receivers(DCR) is given. Also addressed is the design of a cross-coupled LC voltage-controlled oscillator (VCO). For the low noise amplifier, which presents major noise contribution to the downconversion receiver front-end, an optimization technique which employs both a parallel capacitance and an interstage inductor is proposed. The addition of this capacitance helps keep the active device relatively small, and the analysis on the effects of the interstage inductor shows that it helps boost gain of the LNA at the desired operation frequency of 2.4GHz, and offers a lower noise figure. In order to achieve direct downconversion, both a passive switching mixer and an active double-balanced mixer

are presented. The passive switching mixer helps solve the problem of flicker noise, but suffers power loss, while the double-balanced architecture helps relieve the problems of DC offset and second-order distortion. The last part of this presentation is about a partially tunable CMOS LC-VCO which achieves good phase noise performance at the cost of smaller tuning range. It uses on-chip spiral inductors and junction varactors in the resonant LC-tank. The presented building blocks can be used for a low-power, low-voltage DCR front-end for 802.11b/g applications. It is concluded that direct down-conversion architecture can find its use in low-power, low-cost 802.11b and Bluetooth applications should the circuit design make use of the optimization techniques addressed in this work.

CHAPTER 1. INTRODUCTION

Radio frequency (RF) integrated circuits have had, in the last few years, one of the greatest improvements in IC marketing, thanks to the fast developing mobile and wireless applications in communication, networking, and entertainment industries. The call for lower cost, lower power consumption, wider bandwidth and higher insensitivity, along with advances in semiconductor processing technology, has made it possible to design a fully integrated RF part [1]. The most widely used radio receiver architecture is the superheterodyne architecture [2], shown in Figure 1.1, that can be dated back to as early as 1918 [3]. In such an architecture, the input RF signal is first applied to a low-noise amplifier (LNA) at RF, then down-converted to an intermediate frequency (IF) by mixing with a local oscillating (LO) signal, then this IF signal is applied to an IF bandpass filter, and then finally mixed with a second LO signal to reach baseband. This architecture can provide sufficiently low noise figure, but its drawback is also evident. It requires an image rejection filter, an IF filter, and at least two LOs, which not only adds to receiver size, but also increases power dissipation. It is therefore natural to turn to another architecture: zero-IF down-conversion, or direct down-conversion. A typical direct down-conversion receiver architecture is shown in Figure 1.2 [4]. In such an architecture, the IF frequency is reduced to zero, thus eliminating the image rejection filter, the IF filter, and also the first LO. The reason is that the phase of the LO with respect to the incoming RF signal is important. If the phases are coincident or anticoncident, the demodulated signal is of maximum strength. If the phase relationship happens to be a quadrature one, the demodulated signal is zero. What remain now are only an

LNA, a conversion mixer, an LO and a baseband lowpass filter (LPF), thus significantly reducing the receiver size and power dissipation. Depending on the requirement of system, an analog/digital converter (ADC) can also be included in this architecture. For this reason, direct conversion technique has seen more and more attention recently, especially for modern wireless application such as GSM/UMTS [5], Wideband CDMA [6], EPRS [7], etc.

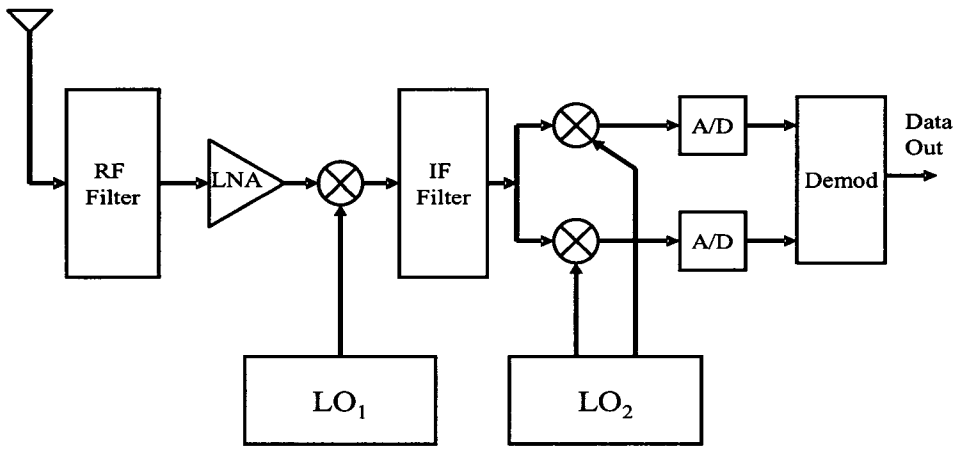

Figure 1.1 Block diagram of a superheterodyne receiver

However, there are also some drawbacks in direct conversions in spite of a considerable number of earnest attempts. These impediments have thus far stymied efforts to use this architecture for more sophisticated applications. Among these problems is an unfortunate, extreme sensitivity to DC offsets and flicker noise. With a zero IF, offsets and flicker noise represent error components within the same band as the desired signal. Another difficulty is intolerance of front-end nonlinearity. Any even-order distortion pro-

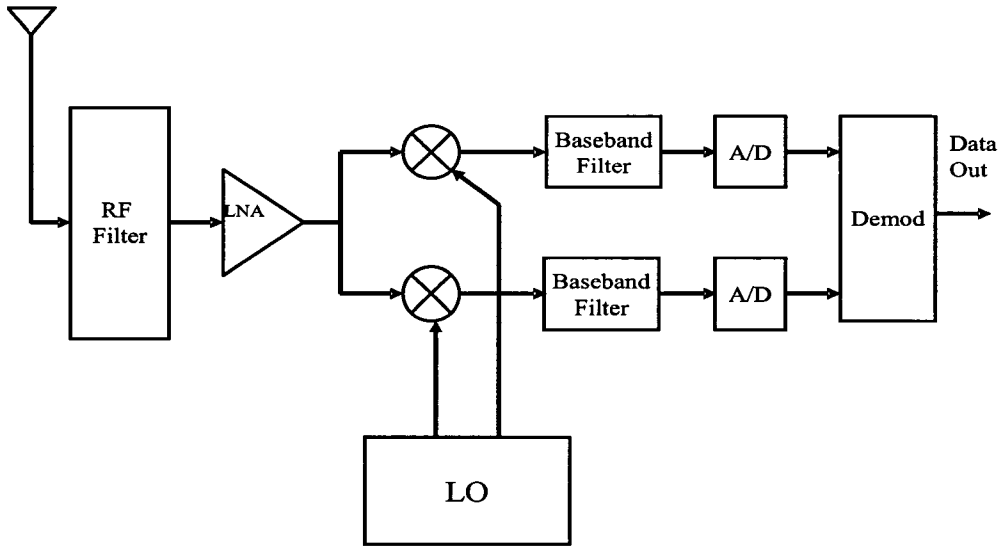

Figure 1.2 Block diagram of a superheterodyne receiver

duces a DC offset that is signal-dependent, and thus represents another "noise" term. This requires that the front-end LNA must be designed to have very high second-order input interception point, or IIP2. This requirement usually forces a significant increase in front-end power dissipation since increasing bias level improves linearity. The third difficulty is that of LO radiation. Since the LO is at the same frequency as that of the RF input signal, LO energy can find its way to the antenna and radiate, causing interference to other receivers, as shown in Figure 1.3. What is worse is that the LO can cause interference to its own receiver. Depending on the phase relationship between the LO signal and the RF signal, as well as the LO component which appears at the RF port, another DC "noise" component will appear in the baseband signal as a result of the mixing action. Since the LO power is generally stronger than that of the RF signal, this self-mixing of LO energy is a significant problem. Extraordinary isolation therefore

must be achieved to prevent the DC offset from dominating the output of the mixer. In summary, the direct-downconversion receiver needs an exceptionally linear LNA, two exceptionally linear mixers, two LO's operating at or near the RF, a method for obtaining a quadrature relationship between the two LO signals, extraordinary isolation of the energy from the LO's and a method for achieving very small offsets and flicker noise. In practice, these goals can not be achieved simultaneously, so a good design is that one can tradeoff them according to design requirements.

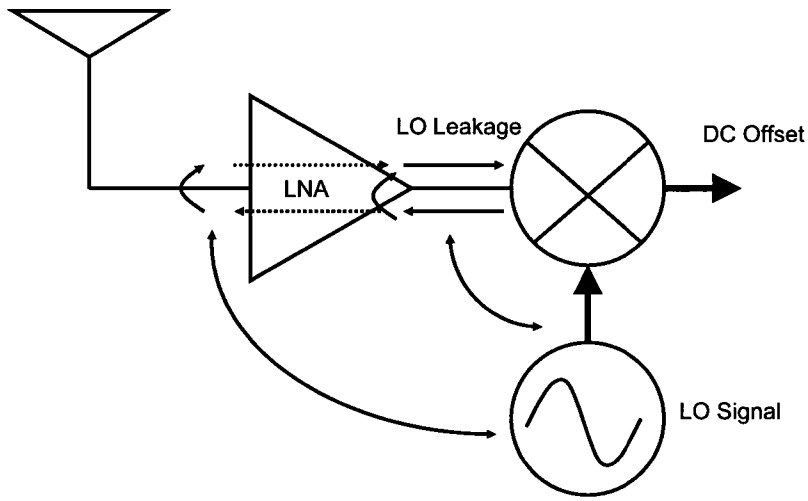

Figure 1.3 LO leakage

Some important issues and challenges in DCR design will be explored more in following sections of this chapter, and a brief introduction of WLAN systems is presented in Chapter 2. In Chapter 3, a noise analysis of LNA is described first, followed by a proposed architecture with a parallel intrinsic capacitance and an interstage inductor, and then simulation results are shown at the end of this chapter. In Chapter 4, two different architectures of direct downconversion mixers are compared with literature reviews, and in Chapter 5, a design of a low voltage cross-coupled LC VCO is introduced. Chapter 6

gives the conclusion of what is presented in this dissertation, and gives a hint on what future work can be done following this work.

1.1 Noise in RF Receivers

One of the most important factors to consider in evaluating the performance of a communication system is its ability to process low-amplitude signals. Every system creates noise, which limits its ability to process weak signals. The principal noise sources are: (1)random thermal noise generated in the resistors and transistors [8]; (2)the undesired cross-coupling of signals between two sections of the receiver, and (3)power-supply noise. Except for thermal noise, all of these sources of noise can be eliminated theoretically, by proper design and construction.

Thermal noise is inherent in all resistors and transistors. It is a critical factor in the performance of communication receivers since it determines the minimum signal level that can be detected. A measure of receiver performance, referred to as noise figure, has long been used to quantitatively describe the noise generated in a communication network.

1.1.1 Thermal Noise

Thermal noise is also called Johnson noise [9] or Nyquist noise [10]. It is cause by thermal vibration of bound charges and thermal agitation of electrons in a conductive material. It exists in all practical passive or active devices. For a resistor which has a resistance of R, its available noise power up to moderately high frequencies has been shown by Nyquist to be [10]:

$$P_N = kTB \tag{1.1}$$

where $k = 1.374 \times 10^{-23} J/K$ is Boltzmann's constant, T is the resistor's physical temperature in Kelvin, and B is its bandwidth.

Because the noise power does not depend on the center frequency of operation but only on the bandwidth, it is called "white noise", as shown in Figure 1.4. A couple of observations about P_N are worth considering:

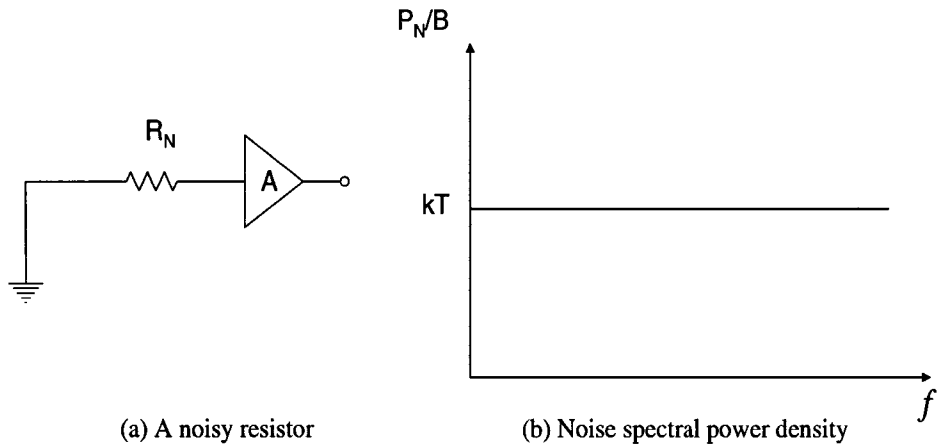

Figure 1.4 White noise in an amplifier

- As bandwidth is reduced, so is P_N, which means narrower bandwidth circuits are less noisy.
- As T is reduced, P_N is also lessened, which means cooler devices generate less noise power.

From above, a noisy resistor R_N at a temperature T can be modelled by an ideal noiseless resistor R_{N0} at 0^0K in conjunction with a noise voltage source $V_{n,rms}$, as shown in Figure 1.5.

From this model, the available noise power to the load under matched condition is given by

$$P_N = \frac{V^2{}_{n,rms}}{4R_N} \tag{1.2}$$

thus

$$V_{n,rms} = 2\sqrt{P_N R_N} = 2\sqrt{kTBR_N} \tag{1.3}$$

From Equation(1.3), one can observe that the noise voltage is proportional to ${R_N}^{1/2}$. Thus, higher-valued resistors have a higher noise voltage even though they provide the

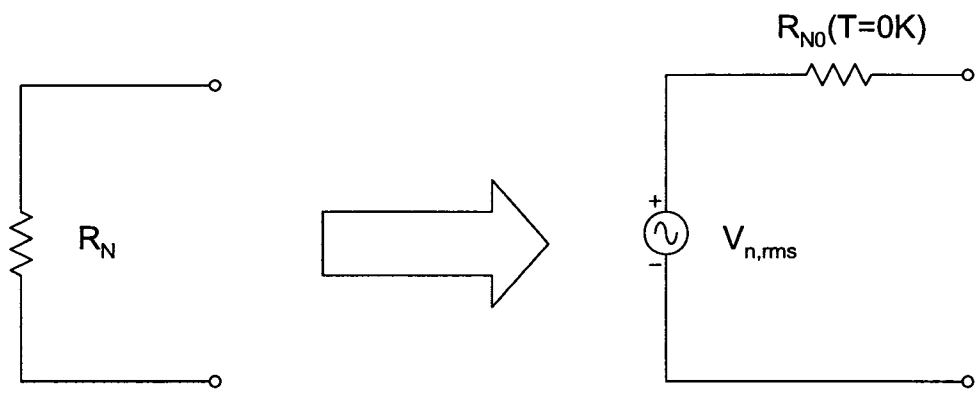

Figure 1.5 Model of a noisy resistor

same noise power level as the lower-valued resistors.

1.1.2 Noise Figure

In many analog circuits, the signal-to-noise-ratio (SNR), defined as the ratio of the signal power to the total noise power, is an important parameter. However, in RF design, a concept of "noise figure" is widely used to characterize receiver front-end's noise performance [11]. The most commonly accepted definition of noise figure represents the ratio of available noise power out of a two-port network divided by the product of available noise power at the input from the source times available gain of the two-port [12]:

$$NF = \frac{P_{No}}{P_{Ni}G_a} \tag{1.4}$$

The available gain G_a is the ratio between available power at the output P_{So} and available power at the input P_{Si}:

$$G_a = \frac{P_{So}}{P_{Si}} \tag{1.5}$$

therefore we have:

$$\begin{aligned} NF &= \frac{P_{No}}{P_{Ni}}\frac{P_{Si}}{P_{So}} = \frac{P_{Si}/P_{Ni}}{P_{So}/P_{No}} \\ &= \frac{SNR_i}{SNR_o} \end{aligned} \tag{1.6}$$

So noise figure can also be defined as the ratio between the input SNR and the output SNR. It is always a number greater than 1. In practice, the noise figure is normally expressed in dB as:

$$NF_{dB} = 10log_{10}(NF) \tag{1.7}$$

In this dissertation, unless otherwise explained, NF is used to denote noise figure in dB.

1.1.3 Noise Figure of Cascaded Stages

For a communication system consisting of cascaded stages, as shown in Figure 1.6, the overall noise figure can be obtained in terms of the noise figure and gain of each stage[11]:

$$NF = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \cdots + \frac{NF_m - 1}{G_1 \cdots G_{(m-1)}} \tag{1.8}$$

Equation 1.8 tells us that the overall noise performance is mainly dominated by that of its first stage, as long as all stages contributes significant positive gains. For a RF receiver front-end, the noise performance of the LNA is extremely important, as it determines the overall noise performance that a front-end can achieve. For example, if an LNA has a noise figure of $2dB$, a gain of $12dB$, and its subsequent mixer has a noise figure of $10dB$, then the front-end consisting of this LNA and this mixer has a noise figure of

$$NF = 10^{\frac{2}{10}} + \frac{10^{\frac{10}{10}} - 1}{10^{\frac{12}{10}}}$$

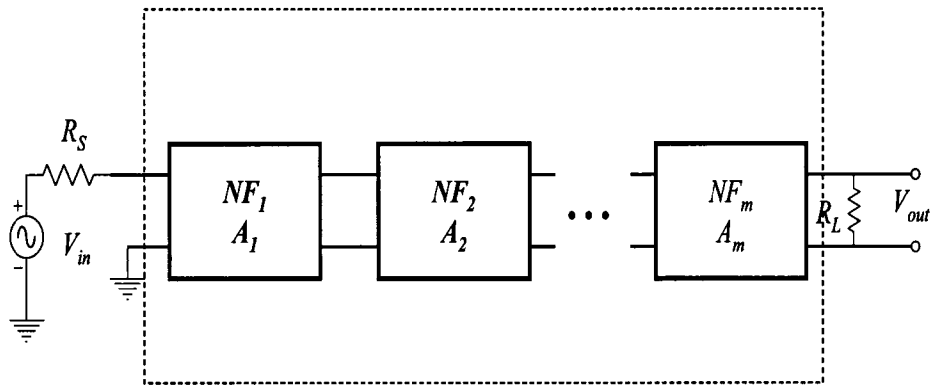

Figure 1.6 Cascaded stages

$$= 2.15$$

$$= 3.33dB \tag{1.9}$$

That's only $1.33dB$ more than the noise figure of the LNA. Also one can find that the higher gain the first stage has, the better noise performance the whole system presents.

1.2 Dynamic Range

Dynamic Range (DR) is generally defined as the ratio of the maximum input level that the circuit can tolerate to the minimum input level at which the circuit can provide a reasonable signal quality [13]. This definition is quantified in different applications differently. For example, in analog circuits such as op amps and analog-to-digital converters, the dynamic range is defined as the ratio of the "full-scale(FS)" input level to the input level for which $SNR = 1$. The full scale is typically the input level beyond which a hard saturation occurs and can be easily found by examining the circuit, and the minimum input level is determined by the noise floor.

In RF design, on the other hand, the situation is more complicated. It is difficult to define the input full scale even for a simple common-source stage. It is possible to define the FS as the input voltage for which the transistor is at the edge of triode region. However, if a sinusoid with a full-scale swing is applied to the circuit, the output exhibits substantial distortion. Also, the minimum signal must provide SNR greater than unity. For these reasons, the definition of the upper end of the dynamic range is based on the intermodulation behavior and the lower end on the sensitivity.

1.2.1 Spurious-Free Dynamic Range

The upper end of the dynamic range is defined as the maximum input level in a two-tone test for which the third-order IM products do not exceed the noise floor. When expressing all of the quantities in dBm, we can write:

$$P_{IIP3} = P_{in} + \frac{P_out - P_{IM,out}}{2} \tag{1.10}$$

where P_{IIP3} is the power at the input third-order interception point, $P_{IM,out}$ denotes the power of $IM3$ components at the output. Since

$$P_{out} = P_{in} + G \tag{1.11}$$

$$P_{IM,out} = P_{IM,in} + G \tag{1.12}$$

where G is the circuit's power gain in dB and $P_{IM,in}$ is the input-referred level of the $IM3$ products, we have

$$\begin{aligned} P_{IIP3} &= P_{in} + \frac{P_out - P_{IM,out}}{2} \\ &= \frac{3P_{in} - P_{IM,in}}{2} \end{aligned} \tag{1.13}$$

so

$$P_{in} = \frac{2P_{IIP3} + P_{IM,in}}{3} \tag{1.14}$$

The input level for which the IM products become equal to the noise floor is thus given by

$$P_{in,max} = \frac{2P_{Ip3} + F}{3} \tag{1.15}$$

where $F = -174dBm + NF + 10logB$ is the noise floor with a noise figure of NF and a bandwidth of B.

The spurious-free dynamic range (SFDR) is the difference (in dB) between $P_{in,max}$ and $P_{in,min}$:

$$\begin{aligned} SFDR &= \frac{2P_{IIP3} + F}{3} - (F + SNR_{min}) \\ &= \frac{2(P_{IIP3} - F)}{3} - SNR_{min} \end{aligned} \tag{1.16}$$

SFDR represents the maximum relative level of interferers that a receiver can tolerate while producing an acceptable signal quality from a small input signal level.

1.2.2 $1dB$ Compression Point

The $1dB$ compression point is another important quantity widely used to characterize a RF circuit's dynamic range. It is defined as the point (on the P_{out} versus P_{in} plot) at which the power gain of the circuit, due to device nonlinearities, is reduced by $1dB$

from its small signal linear power gain value, i.e.,

$$G_{1dB} = G_0 - 1 \tag{1.17}$$

where G_0 is the small signal linear power gain in dB.

If we designate the input power at the $1dB$ gain compression point as $P_{in,1dB}$ and the output power as P_{1dB}, as shown in Figure 1.7, then we can write:

$$G_{1dB} = \frac{P_{1dB}}{P_{in,1dB}} \tag{1.18}$$

or

$$P_{1dB}(dBm) = P_{in,1dB}(dBm) + G_{1dB}(dB) \tag{1.19}$$

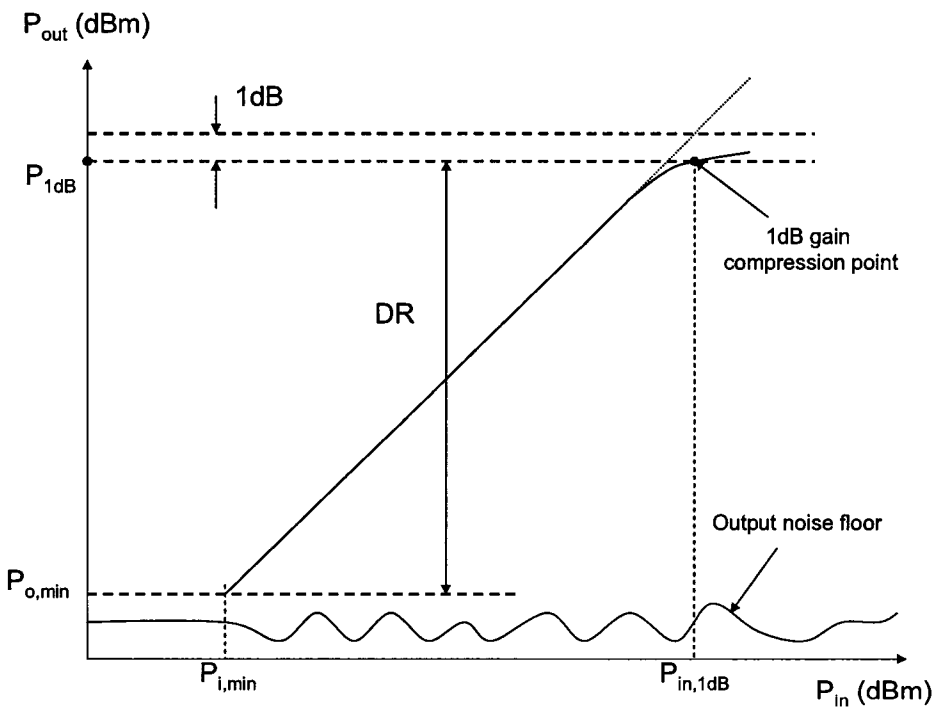

Figure 1.7 The definition of 1dB gain compress

1.2.3 Third-Order Intercept Point

When two or more signals at frequencies f_1 and f_2 are applied to a nonlinear device, they generate intermodulation (IM) products with frequencies of $mf_1 \pm nf_2$ (where $m, n = 0, 1, 2, ...$). These may be the second-order $f_1 \pm f_2$ products, third-order $2f_1 \pm f_2$, $2f_2 \pm f_1$ products, etc. The two-tone odd-order IM products are of primary interest since they tend to have frequencies that are within the passband of desired signal frequency range.

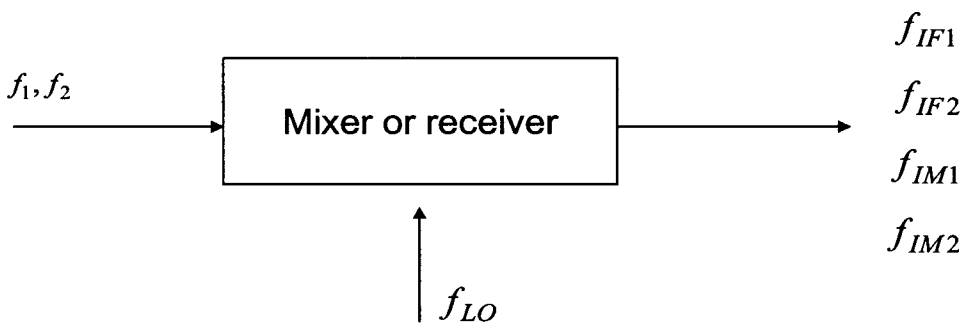

Figure 1.8 Signals generated from two RF tones

Consider a mixer or a receiver as shown in Figure 1.8. f_{IF1} and f_{IF2} are desired IF outputs, andf_{IM1} and f_{IM2} are the third-order IM (IM3) products that also appear at the output port. The IM3 products are generated from f_1 and f_2 mixing with one another and then beating with the mixer's local oscillator according to the expressions

$$(2f_1 - f_2) - f_{LO} = f_{IM1} \tag{1.20}$$

$$(2f_2 - f_1) - f_{LO} = f_{IM2} \tag{1.21}$$

f_{IM1} and f_{IM2} are shown in Figure 1.9 with IF products of f_{IF1} and f_{IF2} generated by the mixer or receiver. These are called third-order products because the coefficients of the $f_1 + f_2$ terms add to three.

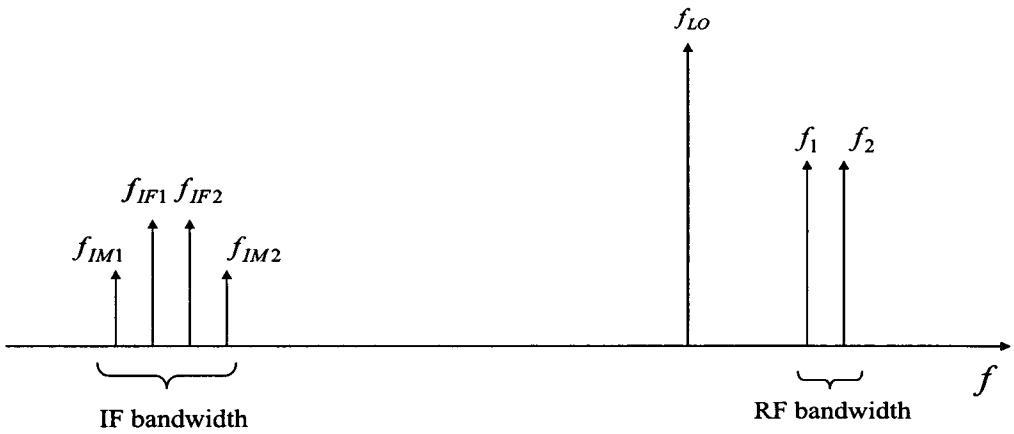

Figure 1.9 Intermodulation products

Note that the frequency separation is

$$\delta = f_1 - f_2 = f_{IM1} - f_{IF1} = f_{IF1} - f_{IF2} = f_{IF2} - f_{IM2} \tag{1.22}$$

These intermodulation products are usually of primary interest because of their relatively large magnitude and because they are difficult or impossible to filter from the desired mixer outputs.

The intercept point, measured in dBm, is a figure-of-merit for intermodulation product suppression. A high intercept point indicates a high suppression of undesired intermodulation products. The third-order intercept point (IP3) is the theoretical point where the desired signal and the third-order distortion have equal magnitudes. The IP3 is an important measure of the system linearity. Typical curves for output power of a fundamental tone and third-order IM products are shown in Figure 1.10. In the linear region, for the IF signals, the output power is increased by $1dB$ if the input power is increased by $1dB$, while the $IM3$ products are increased by $3dB$ for a $1dB$ increase in P_{in}. The slope of the curve for the $IM3$ products is 3:1.

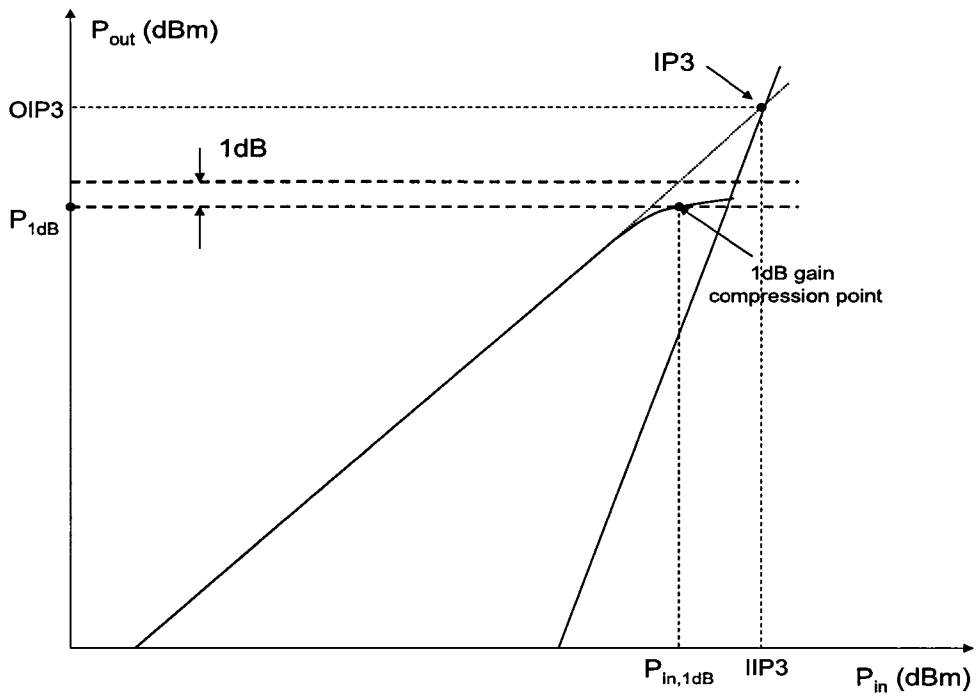

Figure 1.10 Illustration of IP3 and 1dB compression point

1.3 Challenges in DCRs

1.3.1 Second-Order Distortion

Second-order distortion in receivers is a type of harmonic distortion. The concept of harmonic distortion has been well explored [14]. Most circuit simulation tools are able to simulate harmonic distortion. Volterra series analysis [15] is a well-established analysis method for harmonic distortion.

In a receiver context, the main problem of second order distortion is its creation of a spurious baseband signal. Consider a general modulated signal, $x(t) = a(t)cos(2\pi f_c t + \theta(t))$, described by its time-varying envelope $a(t)$ and its instantaneous phase $\theta(t)$. This signal is input to a system with second-order distortion. Apart from the desired signal, such a system also has the response $y(t) = x^2(t)$. The output is

$$y(t) = x^2(t) = \frac{1}{2}a^2(t)(cos(4\pi f_c t + 2\theta(t)) + 1) \tag{1.23}$$

The output of this system is a sum of a high frequency component and a baseband signal which is proportional to the instantaneous signal envelop power. This spurious baseband signal can be large compared to the desired signal, if the desired input signal is weak and the interfering signals are large, which is often the case in RF receivers.

In a direct downconversion receiver, there are two sources of second-order distortion [16]:

- Device nonlinearity such as the quadratic behavior of a MOS transistor.
- Crosstalk between the RF and LO ports.

Using Volterra series analysis [15], it can be shown that a perfectly balanced circuit compensates any even-order, including second-order, distortion [14]. Because a balanced circuit is simple to design and effective, the use of balanced circuits is a preferred solution for reducing second-order distortion. The amount of reduction that a balanced circuit

provides is limited by the matching of the two signal paths and to the amplitude balance of the input signal. This is exactly the approach that this work is taking in implementing direct downconversion mixers.

Harmonic mixers remove the problems caused by RF-LO crosstalk. They achieve frequency conversion by mixing the desired signal with harmonics of the LO signal. For instance, a perfect second-order harmonic mixer would mix the RF input signal only with the second harmonic of the LO signal. Such a mixer is insensitive to the crosstalk between the RF and LO port. However, second-order distortion products of the RF input signal still exist [18].

1.3.2 DC Offsets

When the RF signal is downconverted to baseband, the band of interest extends to zero frequency and extraneous offset voltage can corrupt the signal and quite possibly saturate the subsequence stages. This problem is more severe in direct downconversion receivers than in any other types of frequency conversions. The major sources of DC offset are shown in Figure 1.11. Whenever a signal is multiplied by itself, it generates a DC component at the output of the mixer. This DC offset can be due to self-mixing of the LO signal, or it can be caused by self-mixing of an interferer. Since the isolation between the LO port and the inputs of the mixer is not infinite, a finite amount of the LO signal is injected to the mixer input and is mixed with itself, creating a DC offset at the output of the mixer. A similar effect occurs when a large interferer is coupled to the LO port of the mixer. The problem is exacerbated in a direct downconversion receiver where interferers can easily find their way to the mixer input [16].

There are various ways to combat the problem of DC offset. The easiest way to eliminate the DC offset is to use capacitive coupling as shown in Figure 1.12(a). Since the signal might contain information at low frequencies, a very low corner frequency is required to minimize the ill effects of capacitive coupling. If the corner frequency is not

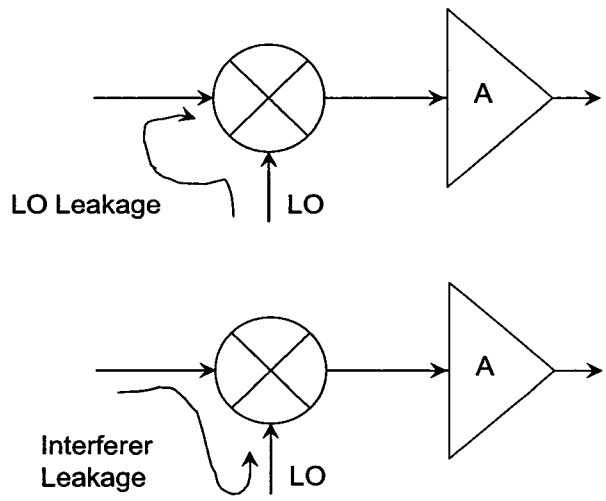

Figure 1.11 Sources of DC offset

low enough, part of the transmitted information is lost. To generate such a low corner frequency, large capacitors are needed. Unfortunately, such large capacitors are hard to build on-chip.

Another approach is to use negative feedback to cancel the DC offset as depicted in Figure 1.12(b). A major advantage of this approach over that in Figure 1.12(a) is that it employs only grounded capacitors and can therefore utilize MOSFETs [17]. Since the capacitance density of MOSFETs is much higher than standard parallel plate structures, this approach has a major area advantage compared to that in Figure 1.12(a). However, the nonlinearity of MOS capacitors can limit the system performance. The high-gain amplifier needed in this approach can also reduce the linearity of the system.

A third approach uses the idle time intervals in digital wireless standards to carry out offset cancellation as shown in Figure 1.12(c). During the idle time intervals, the switch is closed and the offset is measured and stored on the capacitor. However, thermal noise of the switch mandates large values for the capacitor.

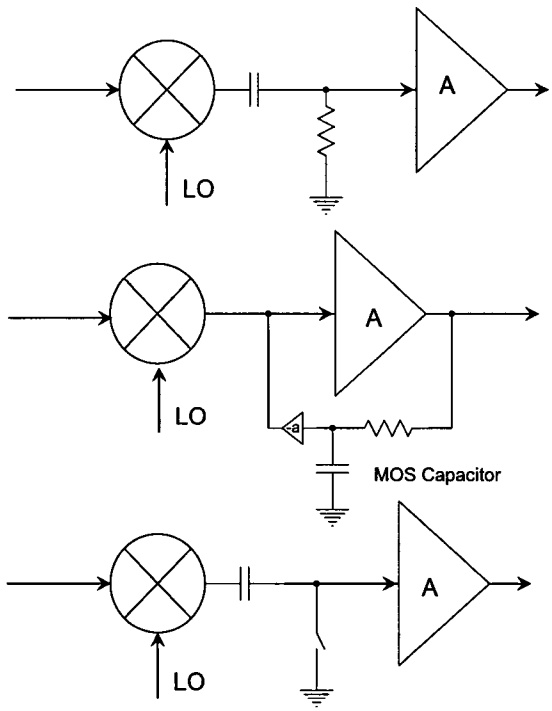

Figure 1.12 DC offset cancellation techniques using (a)capacitive coupling; (b) linear feedback; and (c)sampling

1.3.3 Flicker Noise

Another major challenge in direct downconversion receiver design is the problem of flicker noise, or $1/f$ noise. For modern technologies, and for the minimum gate-length transistors required by RF circuits, the flicker noise component might exceed the white noise up to several megahertz [19].

Flicker noise is not a limiting effect for linear RF circuits, as typically for LNAs, since the operating frequency is much higher than the flicker-noise corner frequency. It can be neglected for baseband processing as well, provided that devices of sufficient active gate area are used. On the other hand, however, the power consumption of the LNA is strongly related to the load it should drive, which is set by the input impedance of the downconverting mixer. In order to keep the receiver front-end power consumption low,

the mixing transistors have to be kept small. Consequently, the flicker noise of these devices is high and tends to corrupt the output baseband signal by degrading the system noise figure. Therefore, the lower the baseband frequency is, the higher the degradation is likely to be, so it is a most important concern for low-power and low-voltage direct-downconversion receivers.

In low-power applications, the LO phase-noise requirement is less stringent than in usual mainstream applications [20]. Therefore, lower LO amplitudes (on the order of 100 to $300mV$) are sufficient, and the power consumption can be lowered. This statement favors the use of mixing devices having the strongest nonlinearity for the smallest possible voltage swing. This condition is fulfilled when the MOS transistors are operated in the weak or moderate inversion region. Because of the downscaling of technologies, this can be realized at frequencies up to a few gigahertz [21].

Another approach that can help relieve the flicker noise problem is to use passive switching mixers. In such a mixer, no DC bias current is needed and the RF signal is directly downconverted to baseband in the voltage domain. Because of the absence of a DC bias current, the flicker noise can be avoided with careful circuit design. This work also uses this approach to address the flicker noise problem.

1.3.4 LO-RF Crosstalk

As described above, LO-RF crosstalk is one of the major contributors to second-order distortion and DC offset. The LO-RF crosstalk results in LO leakage to the LNA and eventually the antenna, whereas the RF-LO crosstalk allows strong interferers in the RF path to interact with the LO signal driving the mixer. Port-to-port isolation is therefore a critical issue in direct downconversion mixer design.

CHAPTER 2. WLAN SYSTEMS

The idea of a modern wireless local area network (WLAN) can be traced back to the late 1970s when IBM laboratories in Ruschlikon, Switzerland reported their infrared (IR) technology for indoor wireless networking [22]. However, the diffuse IR technology never provided a reliable link for desired data rates and suffered from requiring a non-obstructed environment [23]. When the industrial, scientific and medical (ISM) band was released by the FCC in 1985, WLANs entered a new era. The advent of new technologies, new architectures, and the allocation of compatible frequency spectrum stimulated the industry, resulting in the appearance of first generation commercial WLAN products around 1990. The demand for WLAN systems has increased steadily since then. In healthcare industries, WLANs not only facilitate wireless connection of laptops, notebooks, and handhold instruments, but also provide a wireless connection to health monitoring systems. They also allow fast and mobile connections to pharmaceutical and personal healthcare databases. In factory floors, WLANs speed up database access, and allow instant network access for delivery trucks. Educational environments also take advantage of WLANs by providing distant learning through wireless classrooms. Students have access to computational databases and online classes with notebook computers no matter where the students are. By far the biggest market for WLANs is in homes and small offices. Multiple computers, printers, and other peripherals are connected without the need for cumbersome wiring. Additional nodes can be introduced easily without retrofitting the building to provide wired connections. Mobility is of course another big advantage. In conference rooms, information can be transferred between laptops in real

time.

This chapter begins with a review of WLAN network topologies in Section 2.1 . After that, Section 2.2 introduces some of the well known WLAN standards and compares them against one another. Section 2.3 is devoted to discussing the requirements of 802.11b standards in detail. In Section 2.4, the objectives are set for the design of a low-power, low-voltage CMOS direct downconversion receiver for 802.11b applications.

2.1 WLAN Network Topologies

For WLAN systems, there are two different ways to configure a network: infrastructure-based and ad hoc, as shown in Figure 2.1. In an infrastructure network, mobile terminals communicate with the backbone network through an accesspoint (AP). In this configuration, a distribution system interconnects multiple basic service sets (BSSs) through access points to form a single infrastructure network. A mobile terminal can then roam among different BSSs without losing connectivity to the backbone. In an ad hoc con-

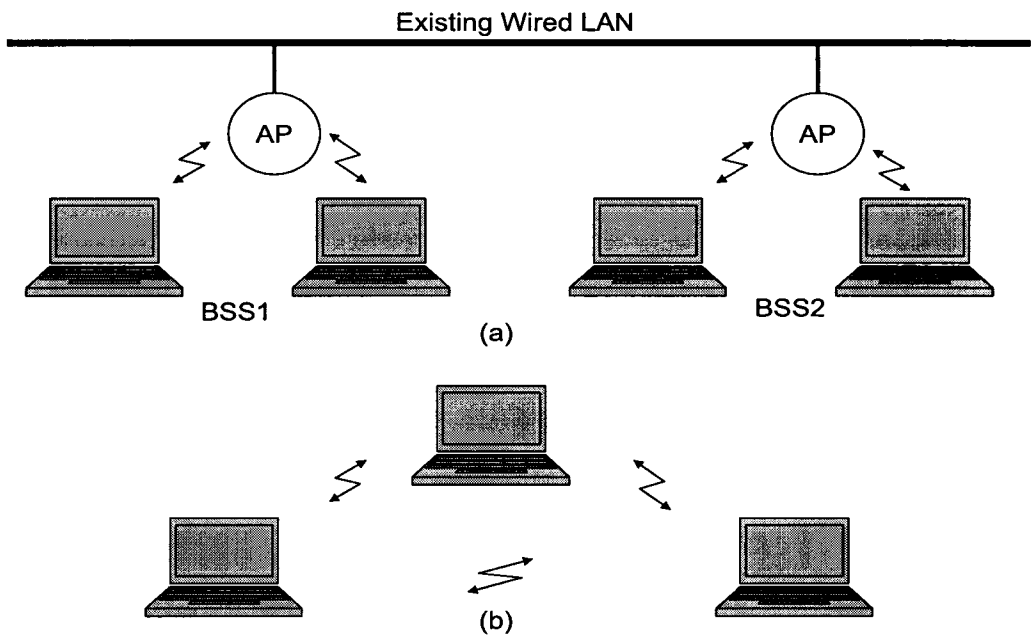

Figure 2.1 Wireless networks: (a) infrastructure-based and (b) ad hoc

figuration, the mobile terminals communicate with each other in an independent BSS without connectivity to the wired backbone. In this topology, computers are brought together to form a network spontaneously and some of the functions of the AP, which are needed to form and maintain a BSS, are provided by one or more of the mobile terminals.

2.2 Overview of WLAN Standards

Wireless can provide a convenient and inexpensive networking solution in a home or an office. However, current wireless standards are as bountiful as they are confusing [24]. Some of the most well known standards for WLAN are summarized in Table 2.1 [24]-[28].

The WLAN interoperability forum (WLIF) advocates its Open-Air standard for small, lightweight, low power mobile data units. It uses the ISM band around $2.4GHz$ to achieve data rates of up to $1.6Mbps$. The HomeRF networking group has produced a set of specifications known as the shared wireless access protocol (SWAP) that uses frequency-hopping (FH) spread spectrum technology in the $2.4GHz$ band to yield data rates of 1 to $2Mbps$. Like HomeRF, Bluetooth is a proposed set of specifications for short-range use within home or office and is fairly inexpensive to implement. It adopts an ad hoc topology and creates piconets. Each piconet consists of up to eight nodes, any of which can be a slave or a master. As a result, Bluetooth is in direct competition with the HomeRF standard, and has dominated it so far. It uses frequently hopping spread spectrum in the $2.4GHz$ ISM band to acheive a $1Mbps$ data rate. It is named after a 10th century Scandinavian king who united several Danish kingdoms.

The IEEE 802.11 standard uses either direct sequence spread spectrum (DSSS), FH spread spectrum, or infrared (IR) pulse position modulation. It makes provisions for data rates of either $1Mbps$ or $2Mbps$ and calls for operation in the ISM frequency band or the infrared band. IEEE 802.11a standard permits data rates of anywhere from 6 to $54Mbps$ using discrete multi-tone (DMT), as well as orthogonal frequency-division multiplexing(OFDM) and operates in the $5GHz$ frequency band. The 802.11b/g standards are a higher-speed version of 802.11b. 802.11b allows data rates of up to $11Mbps$, while 802.11g allows data rates of up to $54Mbps$. As yet none of the existing standards has received universal acceptance. New standards are still under development to achieve better quality of service(QoS), lower system costs, and higher data rates,

Table 2.1 WLAN standards

Designation	Frequency (GHz)	Modulation	Data rate ($Mbps$)
Open-Air	2.4	FH	1.6
HomeRF (SWAP)	2.4	FH	1-2
Bluetooth	2.4	FH	1
802.11	2.4	FH/DSSS	1-2
802.11a	5	DMT/OFDM	6-54
802.11b	2.4	DSSS	11
802.11g	2.4	FH/DSSS	54
DECT	1.9	GFSK	1.152

while operating in a hostile environment in the presence of strong interferers.

2.3 IEEE 802.11b Standard

In 1997, the Institute of Electrical and Electronics Engineers (IEEE) created the first WLAN standard, which was called 802.11 after the name of the group formed to oversee its development. Unfortunately, 802.11 only supported a maximum data-rates of $2Mbps$ - too slow for most applications. For this reason, ordinary 802.11 wireless products are no longer being manufactured.

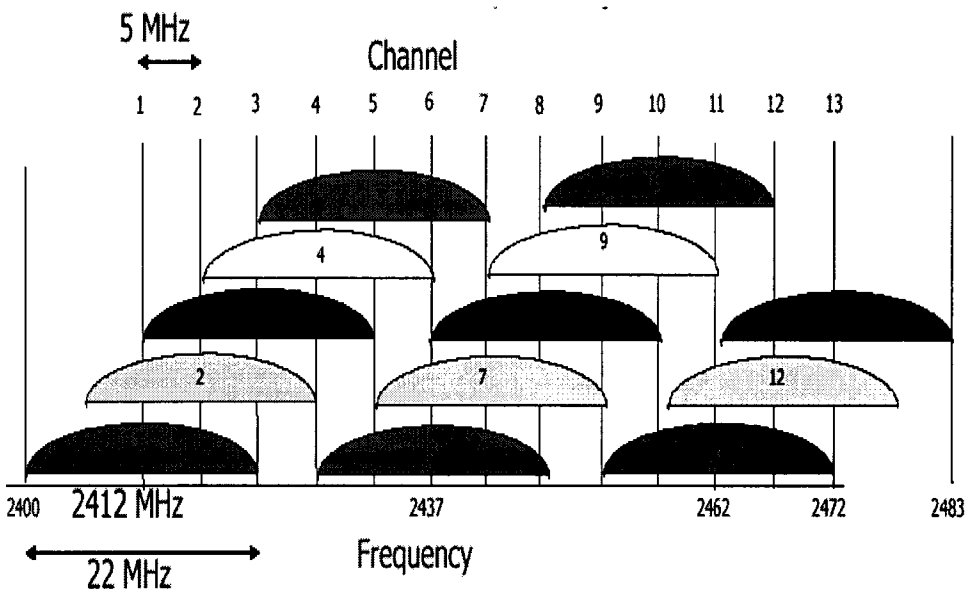

Figure 2.2 The IEEE 802.11b channel plan

In July 1999, IEEE expanded on the original 802.11 standard, creating the 802.11b specification. 802.11b supports bandwidth up to $11Mbps$, comparable to traditional Ethernet. It uses the same radio frequency - $2.4GHz$ - as the original 802.11 standard. Being an unregulated frequency, 802.11b gear can incure interference from microwave ovens, cordless phones, and other appliances using the same $2.4GHz$. However, by installing 802.11b gear a reasonable distance from other appliances, interference can be

Table 2.2 Rate-dependent modulation techniques for the IEEE 802.11b standard

Data rate ($Mbps$)	Modulation
1	DBPSK
2	DQPSK
5.5	CCK
11	CCK

Table 2.3 Sensitivity requirements for the IEEE 802.11b standard

Data rate ($Mbps$)	Sensitivity (dBm)
1	-85
2	-84
5.5	-82
11	-76

easily avoided.

The 802.11b standard uses a direct sequence spread spectrum (DSSS) system with 3 uncorrelated channels and 13 subcarriers as shown in Figure 2.2. Each channel has a bandwidth of $22MHz$, with a $5MHz$ separation between adjacent channels. The DSSS system provides data payload communication capabilities of 1, 2, 5.5 and $11Mbps$. the subcarriers are modulated using Differential Binary Phase Shift Keying(DBPSK), Differential Quadrature Phase Shift Keying(DQPSK) or Complementary Code Keying(CCK) as shown in Table 2.2. The sensitivity requirements of the 802.11b standard are summarized in Table 2.3. The required sensitivity depends on the data rate of the signal, as well as the modulation scheme and the coding technique. To meet the sensitivity requirements for all the various data rates, the 802.11b standard recommends a noise figure of $10dB$ with $5dB$ implementation margins.

The dynamic range of the system depends on the sensitivity of the receiver as well as the maximum signal level that can be successfully decoded. The receiver is required to detect signals as high as -10dBm with less than 8% packet error rate (PER) for a typical sublayer data (PSDU) length of 1024 bytes. The received signal strength (RSS) should be monitored in order to determine if the channel is busy.

2.4 Summary

WLANs allow for easy portable communications and eliminate the problems and costs associated with LAN wiring. The sucess of WLANs involves standardizations to allow seamless interaction between various systems. In this chapter we discussed some of the existing WLAN standards and a summary of their specifications were provided for both low and high data-rate systems. Among the existing standards, the characteristics of the IEEE 802.11b standard were studied in more detail. In the following chapters, we focus on the design and implementation of a low-power, low-voltage direct downconversion CMOS receiver that is compatible with this standard.

CHAPTER 3. LOW NOISE AMPLIFIER

A low noise amplifier (LNA) is the first stage of a receiver frontend, and its noise performance has the most significant effect on that of the whole receiver frontend, so the focus of this dissertation is put on analysis and design of a LNA with super low noise figure.

3.1 Proposed LNA Architecture

The proposed LNA architecture is shown in Figure 3.1. It is a single-stage inductively source degenerated cascode architecture. Transistor $M1$ in a common-source configuration is the amplifying stage, while $M2$ in a common-gate configuration is the cascode stage. On-chip spiral inductor L_s in the source provides degeneration to provide positive components for input impedance. Another inductor L_g is the gate inductance to help input impedance matching. R_{out}, L_{out} and C_{out} consist of an output tank to help output impedance matching. $M3$ is in current mirror configuration with $M1$, which provides bias voltage for the input port together with resistors $R1$ and $R2$. $C1$ and $C2$ are blocking capacitors for input and output ports, respectively. The novelty of this architecture lies in the addition of C_d and L_a. The intrinsic capacitance C_d is put in parallel with the gate-source capacitance C_{gs1} of $M1$, and L_a, also an on-chip spiral inductor, is placed between the common-source stage and the common-gate stage. The addition of both C_d and L_a helps to improve the performance of this LNA, which will be explained below in detail. Before that, a brief introduction of a spiral inductor is presented.

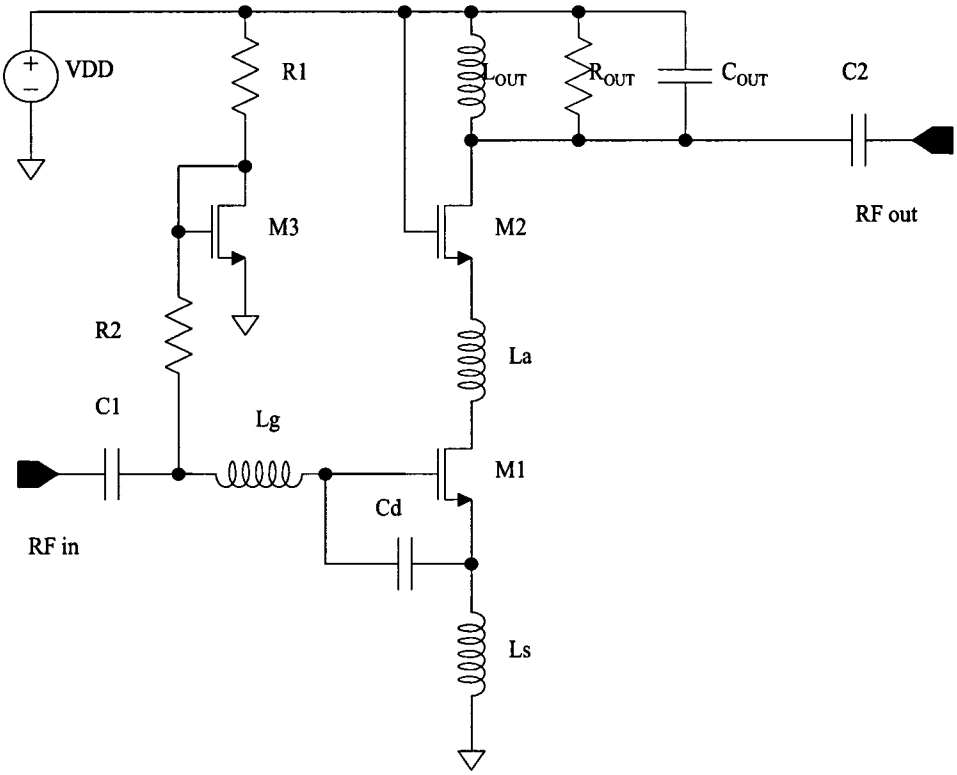

Figure 3.1 Schematic of proposed LNA

3.2 Spiral Inductors

The equivalent circuit model of a spiral inductor is shown in Figure 3.2, where L is the series inductance and R is the RF series resistance of the metal lines [29]. C_s is the series capacitance, C_{ox1} and C_{ox2} are the capacitances between the inductor and the substrate, C_{sub1} and C_{sub2} are the capacitances of the substrate, and R_{sub1} and R_{sub2} are the RF resistances of the substrate. The quality factor of a spiral inductor is defined as the ratio of energy stored in it over energy lost in one oscillation cycle [30]. Metal wire resistance, capacitive coupling to the substrate, and magnetic coupling to the substrate limit the Q-factors of on-chip spiral inductors.

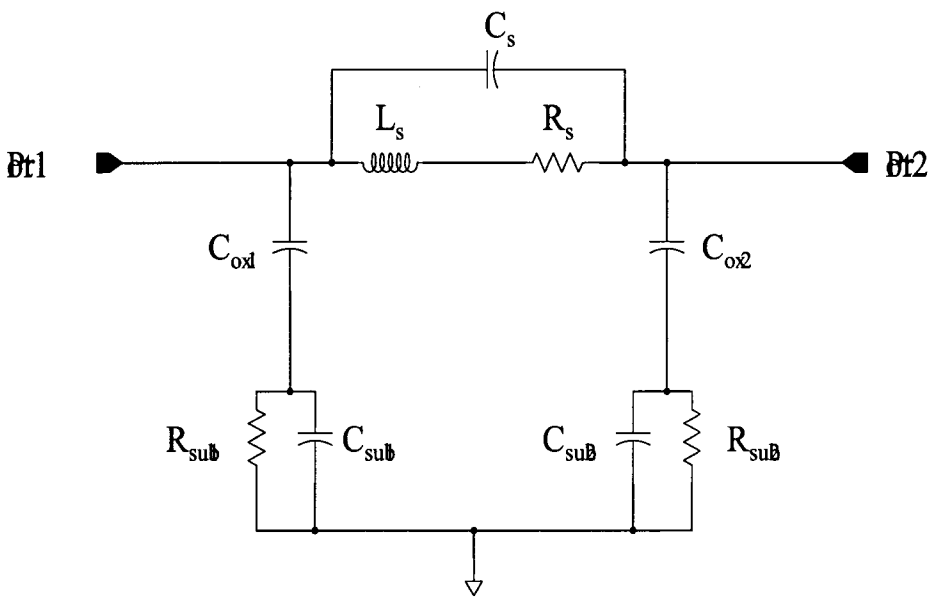

Figure 3.2 Circuit model of spiral inductor

3.3 Impact of C_d

If we ignore L_a and gate-drain capacitance C_{gd} of $M1$, the input impedance of the common-source stage can be expressed as[31],[32]:

$$Z_{in} = j\omega L_t + \frac{1}{j\omega C_t} + R_t + g_{m1}\frac{L_s}{C_t} \tag{3.1}$$

where

$$L_t = L_g + L_s \tag{3.2}$$

$$C_t = C_{gs1} + C_d \tag{3.3}$$

$$R_t = R_g + R_l \tag{3.4}$$

$$R_g = R_o\frac{1}{3n^2}\cdot\frac{W}{L} \tag{3.5}$$

C_{gs1}: Gate-to-source capacitance of M1

g_{m1}:Transconductance of M1

R_g: Effective gate resistance[33]

n: Number of fingers of M1

R_t: Parasitic resistance of L_g and L_s

At the resonance frequency:

$$f_0 = \frac{1}{2\pi\sqrt{L_t C_t}} \tag{3.6}$$

the input matching condition is:

$$R_s = R_t + g_{m1}\frac{L_t}{C_t} \tag{3.7}$$

the quality factor for the input circuit is then

$$Q = \frac{1}{2\pi f_0[R_s + (R_t + g_{m1}\frac{L_s}{C_t})]C_t} \tag{3.8}$$

$$= \frac{1}{4\pi R_s f_0 C_t} \tag{3.9}$$

and the unity gain frequency is:

$$f_T = \frac{g_{m1}}{2\pi C_t} \tag{3.10}$$

and the noise factor of the LNA can be expressed as:

$$F = 1 + \frac{R_t}{R_s} + \gamma g_{d0} R_s (\frac{f_0}{f_T})^2 \tag{3.11}$$

where g_{d0} is the zero-bias drain conductance of M1, and γ is a bias-dependent factor that, for long channel devices, satisfies:

$$\frac{2}{3} \leq \gamma \leq 1 \tag{3.12}$$

It has been found that the dominant term in (3.11) is the last term, which arises from channel thermal noise[34]. By scaling down the width of M1, g_{d0} can be reduced, which implies better noise performance and less power dissipation, provided f_T is maintained. However, scaling down reduces C_{gs1}. If C_d is not added, it will result in an increase of L_t to maintain a constant resonance frequency according to equations (3.6), (3.2) and (3.3). Adding C_d in parallel with C_{gs1} not only keeps C_{gs1} small, which means less gate induced current noise, but also minimizes parasitic effects of L_s and L_g[32].

3.4 Impact of L_a

The position of L_a in this circuit can be illustrated in Figure 3.3. The output impedance of the common-source stage, Z_{out_CSS}, and the input impedance of the common-gate stage, Z_{in_CGS}, are both capacitive without L_a. With the addition of L_a, an intuitive observation is that the positive reactance provided by L_a helps compensate negative reactance of both Z_{in_CGS} and Z_{out_CSS}, which improves matching to get a higher power gain, hence better noise performance. This observation can be explained explicitly as follows.

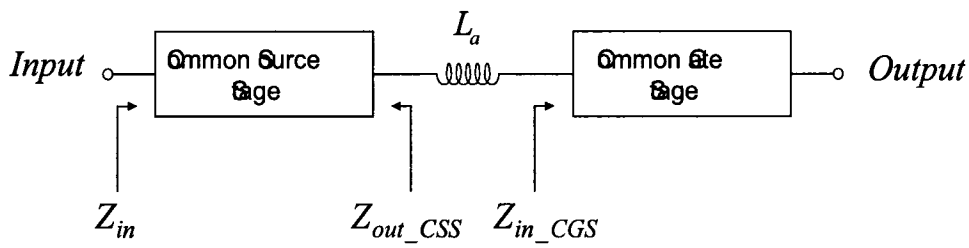

Figure 3.3 Illustration of L_a

In order to investigate the effects of L_a, a small signal model of the LNA is shown in Figure 3.4, where the gate-drain capacitance C_{gd1} and the output impedance r_{ds1} of $M1$ are taken into consideration. C_{s2} represents the summation of the gate-source capacitance C_{gs2} and other parasitic capacitances of the common-gate transistor $M1$, and Z_{out} represents output impedance of $M2$.

The nodal equations at $G1$, $S1$, $D1$, $S2$ and $D2$ can be written as:

$$V_{g1}(y_{in} + sC_{gs1} + sC_{gd1}) - V_{in}y_{in} - V_{s1}(sC_{gs1} + sC_{gd1}) = 0 \tag{3.13}$$

$$V_{d1}(g_{ds1} + sC_{gd1} + \frac{1}{sL_a}) + g_{m1}(V_{g1} - V_{s1}) - V_{g1}sC_{gd1} - V_{s1}g_{ds1} - V_{s2}\frac{1}{sL_a} = 0 \tag{3.14}$$

$$V_{s1}(g_{ds1} + sC_{gs1} + \frac{1}{sL_s}) - V_{d1}g_{ds1} - V_{g1}sC_{gs1} - g_{m1}(V_{g1} - V_{s1}) = 0 \tag{3.15}$$

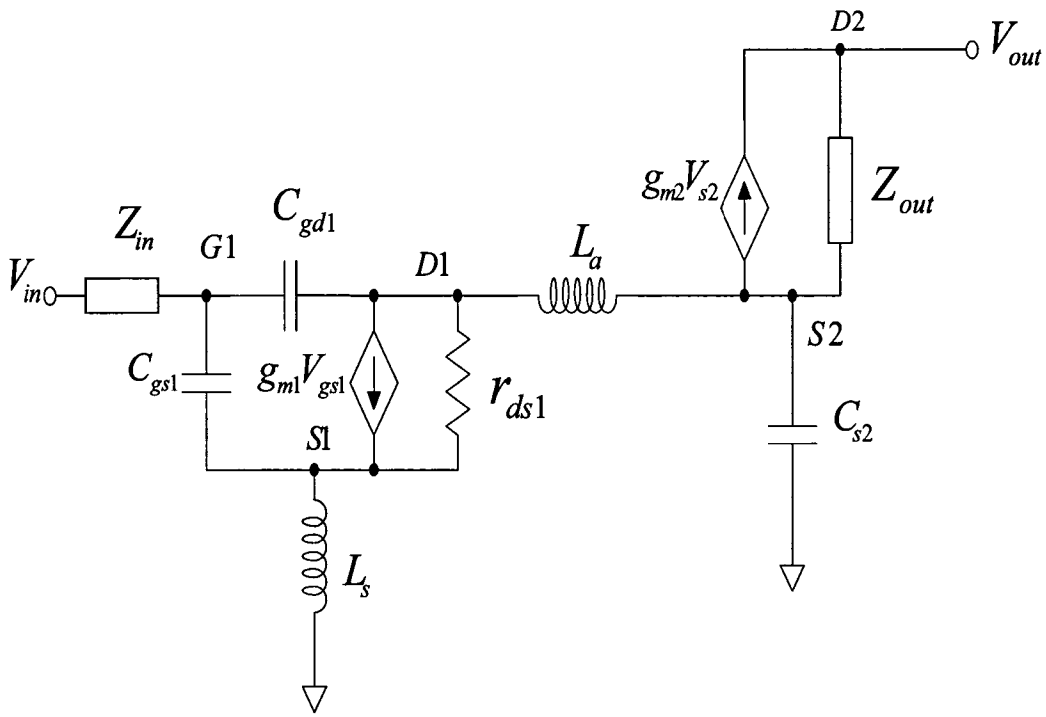

Figure 3.4 Small signal model of the LNA to investigate the effects of L_a

$$V_{s2}(g_{ds2} + y_{out} + sC_{s2} + \frac{1}{sL_a}) + g_{m2}V_{s2} - V_{out}(g_{ds2} + y_{out}) - V_{d1}\frac{1}{sL_a} = 0 \tag{3.16}$$

$$V_{out}(g_{ds2} + y_{out}) - g_{m2}V_{s2} - V_{s2}(g_{ds2} + y_{out}) = 0 \tag{3.17}$$

By solving equations (3.13)-(3.17), the voltage gain A_v can be found to be

$$A_v = V_{out}/V_{in} = \frac{-g_{m1}r_{ds1}(1 + g_{m2}Z_{out}) + E(s)}{F(s)} \tag{3.18}$$

where

$$\begin{aligned} E(s) &= s^2L_s\{C_{gs1}(1 + g_{m2}Z_{out}) + C_{gd1}[g_{m2}Z_{out} + g_{m1}r_{ds1}(1 + g_{m2}Z_{out})]\} \\ &+ sC_{gd1}(1 + g_{m2}Z_{out})(r_{ds1} + s^2C_{gs1}L_s) \end{aligned} \tag{3.19}$$

$$\begin{aligned} F(s) &= s^5 C_{gs1} C_{gd1} C_{s2} L_s L_a + s^4 C_{s2} L_s L_a [C_{gs1} + C_{gd1}(1 + g_{m1} r_{ds1})] \\ &+ s^3 r_{ds1} [C_{gs1} L_s (C_{s2} + C_{gd1}) + C_{s2} C_{gd1} L_a] \\ &+ s^2 \{C_{s2}(L_s + L_a + g_{m1} r_{ds1} L_s) + L_s (C_{gs1} + C_{gd1}(1 + g_{m1} r_{ds1})]\} \\ &+ s r_{ds1}(C_{s2} + C_{gd1}) + 1 \end{aligned} \tag{3.20}$$

What we are interested in is the denominator in (3.18), $F(s)$. It can be rearranged as the summation of a L_a related term and a non-L_a related term, as shown below:

$$F(s) = G(s) + L_a H(s) \tag{3.21}$$

where the non-L_a related term $G(s)$ is:

$$\begin{aligned} G(s) &= s^3 r_{ds1} C_{gs1} (C_{s2} + C_{gd1}) L_s \\ &+ s^2 L_s [C_{gs1} + (C_{s2} + C_{gd1})(1 + g_{m1} r_{ds1})] \\ &+ s r_{ds1}(C_{s2} + C_{gd1}) + 1 \end{aligned} \tag{3.22}$$

and the L_a related term $H(s)$ is:

$$\begin{aligned} H(s) &= s^5 C_{gs1} C_{gd1} C_{s2} L_s + s^4 C_{s2} L_s [C_{gs1} + C_{gd1}(1 + g_{m1} r_{ds1})] \\ &+ s^3 r_{ds1} C_{s2} C_{gd1} + s^2 C_{s2} \end{aligned} \tag{3.23}$$

Let $s = jw$, we have

$$G(jw) = P(w) + jQ(w) \tag{3.24}$$

$$H(jw) = S(w) + jT(w) \tag{3.25}$$

where

$$P(w) = w^4 C_{gd1} C_{s2}(1 + g_{m1} r_{ds1}) + w^2 C_{s2}(w^2 L_s C_{gs1} - 1) \tag{3.26}$$

$$Q(w) = w^3 C_{gd1} C_{s2}(w^2 L_s C_{gs1} - 1) \tag{3.27}$$

$$S(w) = 1 - w^2 L_s [C_{gs1} + (C_{s2} + C_{gd1})(1 + g_{m1} r_{ds1})] \tag{3.28}$$

$$T(w) = w r_{ds1}(C_{s2} + C_{gd1})(1 - w^2 L_s C_{gs1}) \tag{3.29}$$

Then we can rearrange $F(jw)$ as a summation of a real part and an imaginary part as

$$F(jw) = [P(w) + L_a S(w)] + j[Q(w) + L_a T(w)] \tag{3.30}$$

Because at our desired operation frequency f_0,

$$w_0 = 2\pi f_0 << \frac{1}{\sqrt{L_s C_{gs1}}} \tag{3.31}$$

then

$$w_0{}^2 L_s C_{gs1} < 1 < r_{ds1} \tag{3.32}$$

so

$$\begin{aligned} P(w_0) &= w_0{}^4 C_{gd1} C_{s2}(1 + g_{m1} r_{ds1}) + w_0{}^2 C_{s2}(w_0{}^2 L_s C_{gs1} - 1) \\ &= w_0{}^2 C_{s2}[w_0{}^2 C_{gd1}(1 + g_{m1} r_{ds1}) + (w_0{}^2 L_s C_{gs1} - 1)] \\ &= w_0{}^2 C_{s2}[w_0{}^2 (C_{gd1} + L_s C_{gs1}) + (w_0{}^2 C_{gd1} g_{m1} r_{ds1} - 1)] \end{aligned} \tag{3.33}$$

$$Q(w_0) = w_0{}^3 C_{gd1} C_{s2}(w_0{}^2 L_s C_{gs1} - 1) \tag{3.34}$$

$$S(w_0) = 1 - w_0{}^2 L_s[C_{gs1} + (C_{s2} + C_{gd1})(1 + g_{m1} r_{ds1})] \tag{3.35}$$

$$T(w_0) = w_0 r_{ds1}(C_{s2} + C_{gd1})(1 - w_0{}^2 L_s C_{gs1}) \tag{3.36}$$

It is easy to find that $w_0{}^2 C_{gd1} g_{m1} r_{ds1} > 1$, so we have

$$\begin{aligned} P(w_0) &> 0 \\ Q(w_0) &< 0 \\ S(w_0) &< 0 \\ T(w_0) &> 0 \end{aligned}$$

Then

$$\begin{aligned} |F(jw_0)|^2 &= [P(w_0) + L_a S(w_0)]^2 + [Q(w_0) + L_a T(w_0)]^2 \\ &= P^2(w_0) + Q^2(w_0) + L_a{}^2[S^2(w_0) + T^2(w_0)] \\ &+ 2L_a[P(w_0)S(w_0) + Q(w_0)T(w_0)] \end{aligned} \tag{3.37}$$

Since $P(w_0)S(w_0) + Q(w_0)T(w_0) < 0$, so we can see that $|F(jw_0)|$ decreases as L_a increases, which in turn results in an increase in voltage gain(3.18). This conclusion is verified through a SpectreRF simulation by sweeping L_a from $1nH$ to $5nH$, as shown in Figure 3.5.

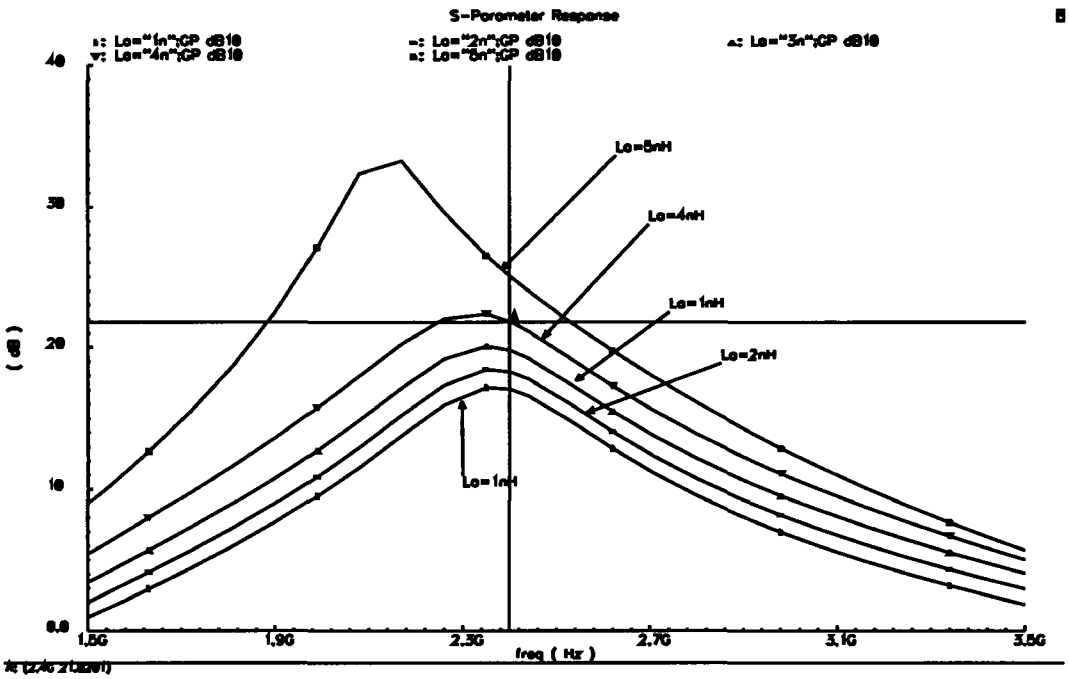

Figure 3.5 S21 vs. L_a

One interesting result from above is the LNA's low-frequency response. At frequencies where the gain has started to decrease but still much greater than unity, the first-order and higher-order terms in the numerator in (3.18) can be ignored. So can the higher-order terms in the denominator. Then we have:

$$\begin{aligned} A_v &= \frac{g_{m1}r_{ds1}(1 + g_{m2}Z_{out})}{1 + s(C_{s2} + C_{gd1})r_{ds1}} \\ &= \frac{A_0}{1 + s(C_{s2} + C_{gd1})r_{ds1}} \end{aligned} \tag{3.38}$$

where the DC gain is:

$$A_0 = g_{m1} r_{ds1} (1 + g_{m2} Z_{out}) \tag{3.39}$$

and the $-3dB$ cutoff frequency is:

$$w_{-3dB} = \frac{1}{(C_{s2} + C_{gd1} r_{ds1}} = \frac{g_{ds1}}{(C_{s2} + C_{gd1})} \tag{3.40}$$

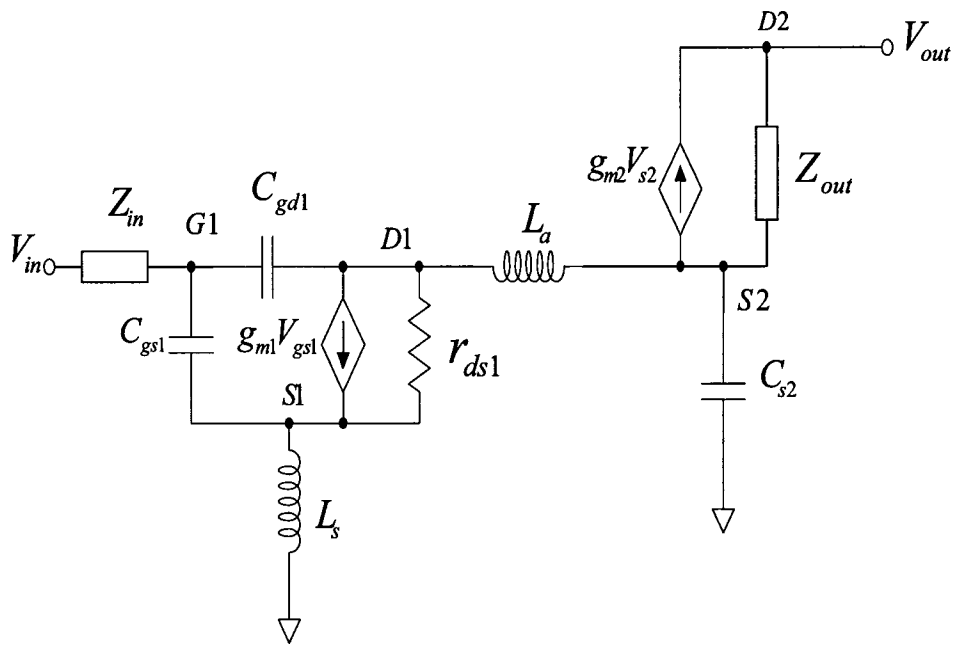

Figure 3.6 Small-signal model to calculate input impedance

Another problem arises as L_a increases: operation frequency shift, as shown in Figure 3.5. This is because the introduction of L_a changes the input impedance of the LNA, and expression (3.1) no longer holds. In order to get a more accurate expression of the input impedance of the LNA, a small-signal model circuit as shown in Figure 3.6 is used to calculate Z_{in}. To make it easier understood, the cascoded common-gate stage is not taken into account, neither is the gate-drain capacitance C_{gd1}. A voltage V_x is applied

at the input port to generate an input current I_x, while the output port is grounded. Similarly, we can write nodal equations at $G1$, $S1$ and $D1$:

$$V_{g1} = V_x \tag{3.41}$$

$$V_{s1}(sC_{gs1} + g_{ds1} + \frac{1}{sL_a}) - g_{m1}(V_{g1} - V_{s1}) - V_{g1}sC_{gs1} - V_{d1}g_{ds1} = 0 \tag{3.42}$$

$$V_{d1}(g_{ds1} + \frac{1}{sL_a}) + g_{m1}V_{gs1} - V_{s1}g_{ds1} = 0 \tag{3.43}$$

$$I_x = (V_{g1} - Vs1)sC_{gs1} \tag{3.44}$$

By solving these nodal equations, we have:

$$\begin{aligned} Z_{in}{}' &= \frac{V_x}{I_x} \\ &= jw[L_s + L_s(L_s + L_a)\frac{g_{m1}g_{ds1}}{C_{gs1}}] + \frac{1}{jwC_{gs1}} + R' \end{aligned} \tag{3.45}$$

It should be noticed Z'_{in} is used instead of Z_{in}. This is because the actual input impedance of the LNA should include the portion contributed by L_g, the gate inductance. Also R' is used to denote all the resistive portion of the input impedance. If we take L_g and C_d into consideration, then the total input impedance of the LNA can be expressed as:

$$Z_{in} = jw[L_t + L_s(L_s + L_a)\frac{g_{m1}g_{ds1}}{C_t}] + \frac{1}{jwC_t} + R] \tag{3.46}$$

where:

$$L_t = L_g + L_s \tag{3.47}$$

$$C_t = C_{gs1} + C_d \tag{3.48}$$

Then the resonance frequency becomes:

$$f_0 = \frac{1}{2\pi\sqrt{L_tC_t + L_s(L_s + L_a)g_{m1}g_{ds1}}} \tag{3.49}$$

at which $Z_{in} = R$ which is the real (resistive) portion of Z_{in}.

It can be been that the presence of the interstage inductance L_a lowers achievable operation frequency f_0 of an LNA, assuming no other changes in the circuitry. f_0 decreases as L_a increases, which explains the frequency shift in Figure 3.5.

3.5 Simulation Results

In the proposed LNA design, a $3.72nH$ *La* is used. The S-parameters of the LNA is plotted in Figure 3.7, and its noise figure is plotted in Figure 3.8. Its performance is summarized in Table 3.1.

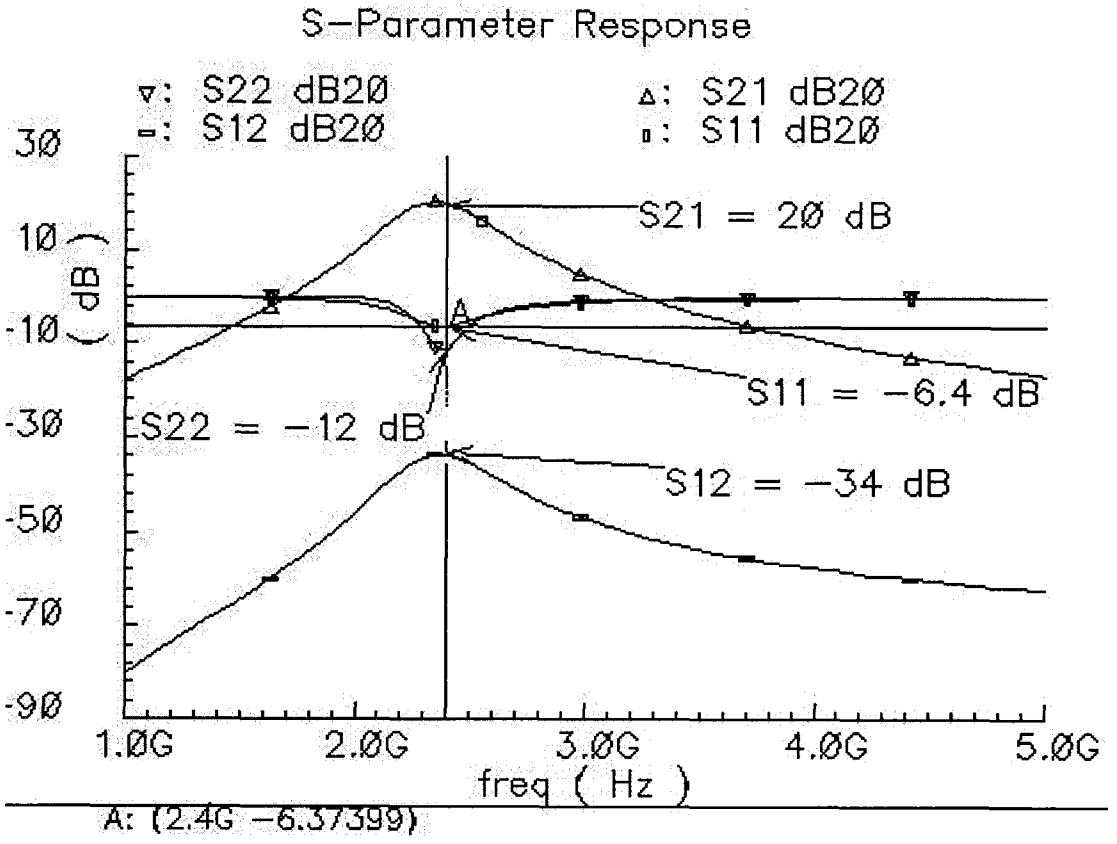

Figure 3.7 S-parameters of the proposed LNA

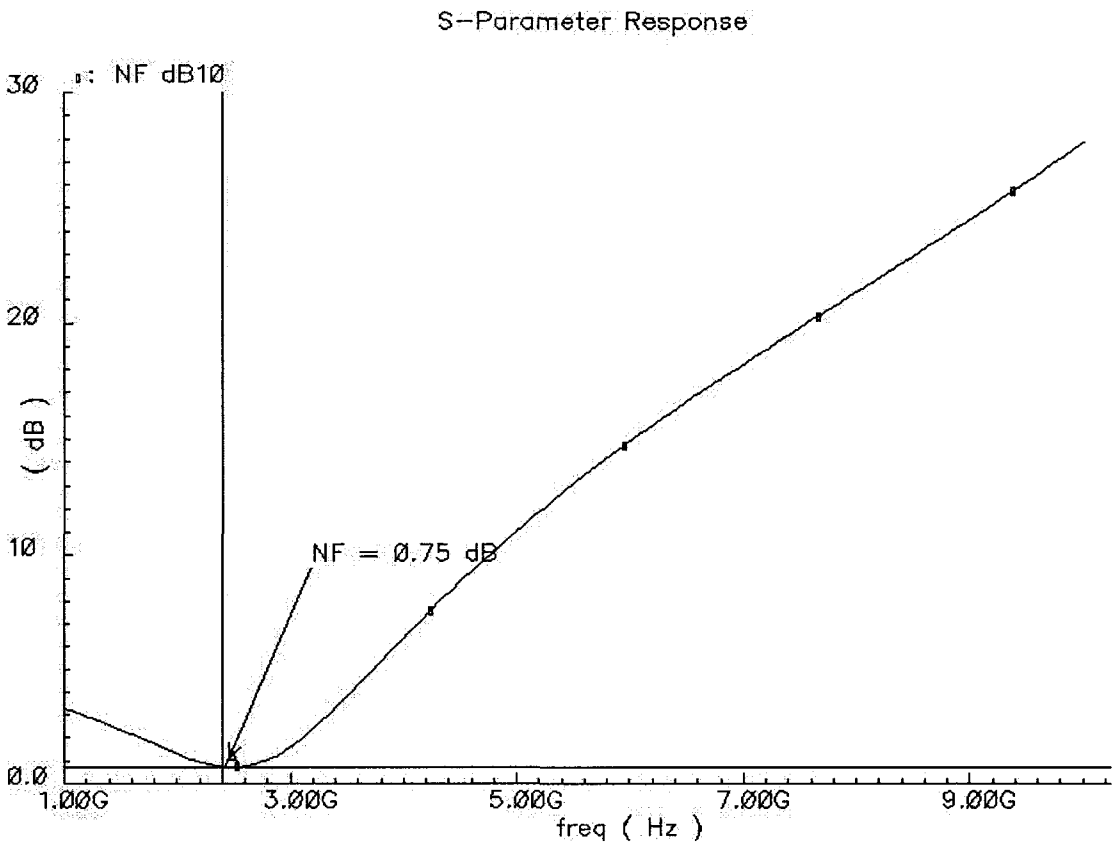

Figure 3.8 Noise figure of the proposed LNA

Table 3.1 LNA performance summary

	This work	[44]	[42]
Process (μm)	0.18	0.18	0.18
Supply voltage(V)	1.2	1.2	1.8
Operation freq.(GHz)	2.4	2.45	2.4
Power dissipation(mW)	2.8	7.76	7.94
Noise figure(dB)	0.75	2.778	4
Power gain(dB)	20	16	12
$S_{11}(dB)$	-6.4	N/A	-10
$S_{12}(dB)$	-34	-30	N/A
$S_{22}(dB)$	-12	N/A	-11

CHAPTER 4. DESIGN OF MIXERS

4.1 Introduction

The mixer is one of the most critical building blocks in modern radio frequency (RF) wireless communication systems. As a part of RF front-end circuits, its performance directly impacts the whole system's performance. Compared with traditional super-heterodyne conversion architecture[34], direct conversion has the potential for reduced power consumption, multi-band operation, reduced dependence on off-chip filters, higher levels of integration and reduced system complexity[33]. However, direct conversion also presents four design challenges: DC offsets, even-order distortion, I/Q mismatches and flicker noise[33]. Careful attention must be taken on these issues during component and system design. For high-speed wireless communications like 802.11b applications, overall radio performance is more dependant upon noise than linearity.

Two mixers are presented in this dissertation: one is a passive switching mixer, the other is an active Gilbert cell-based direct downconversion mixer, while both are implemented in a 6-metal-1-poly $0.18\mu m$ CMOS process. For the switching mixer, the switching process is directly in the voltage domain, while for the active mixer, the switching process is realized by the active devices driven by a $2.4GHz$ sinusoid LO signal with a power level of -$10dBm$. An input matching network at the RF input port is used to improve the mixer's performance.

4.2 Switching Mixer

In typical active Gilbert-type mixers, the RF signal is represented in the form of current instead of the RF voltage itself. The V-I conversion is realized by multiplying

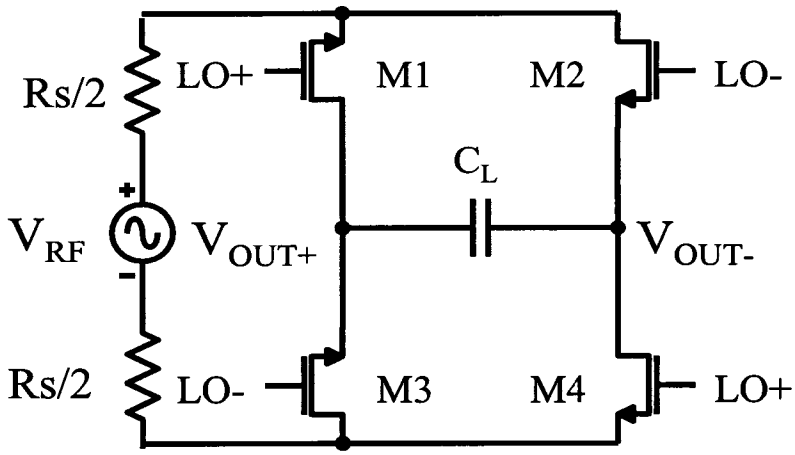

Figure 4.1 A simple double-balanced CMOS switching mixer

it with a square-wave version of the local oscillator. In order to avoid the V-I conversion problem, an alternative is to switch the RF signal directly in the voltage domain. Since CMOS transistors are excellent switches themselves, high-performance passive switching mixers can be realized effectively with CMOS technology. A simple double-balanced passive switching mixer is shown in Fig. 4.1, which consists of four transistors in a bridge configuration. The four transistors operate as switches connecting either the RF signal or the inverse of the RF signal to the output terminal driven by the local oscillator signal. A general expression of the output of the mixer is given in [31], which is expressed as the product of three time-varying components and a scaling factor:

$$v_{OUT}(t) = v_{RF}(t) \cdot [\frac{g_T(t)}{g_{T_{max}}} \cdot m(t)] \cdot [\frac{g_{T_{max}}}{\overline{g_T}}] \tag{4.1}$$

where $g_T(t)$ is the time-varying Thevenin-equivalent conductance as viewed from the output port, and $g_{T_{max}}$ and $\overline{g_T}$ are the maximum and average values, respectively, of $g_T(t)$. The mixing function $m(t)$ is defined by:

$$m(t) = \frac{g(t) - g(t - \frac{T_{LO}}{2})}{g(t) + g(t - \frac{T_{LO}}{2})} \tag{4.2}$$

where $g(t)$ is conductance of each switch and T_{LO} is the period of the LO drive. It can be observed that the mixing function has no DC component and has only odd harmonic content because of its half-wave symmetry.

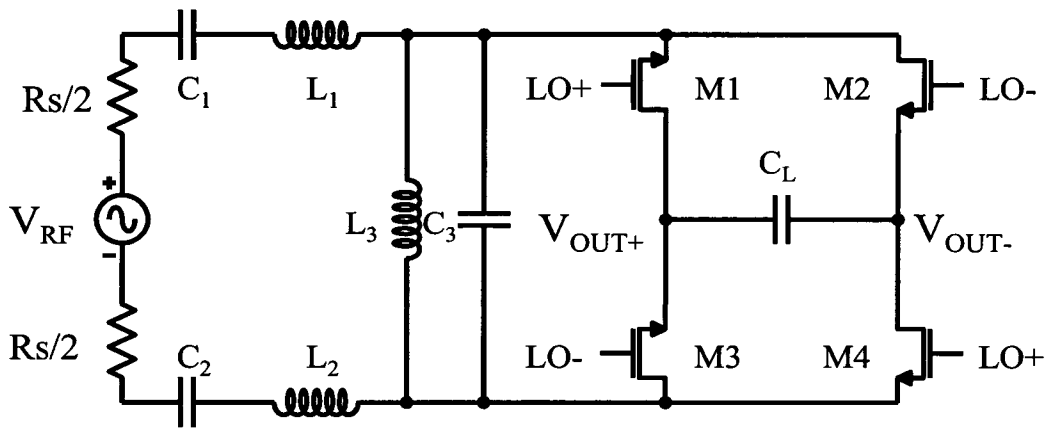

Figure 4.2 A switching direct downconversion mixer with impedance transformation [31]

A widely-used switching mixer is shown in Fig. 4.2[31]. C_1 and L_1 together with C_3+L_3 provide an impedance transformation, and L_3 and $C_3 + C_L$ form a parallel tank

which acts as a bandpass filter. Because of the absence of DC bias current in this mixer, the flicker noise is absent, which makes it particularly valuable for direct downconversion receivers.

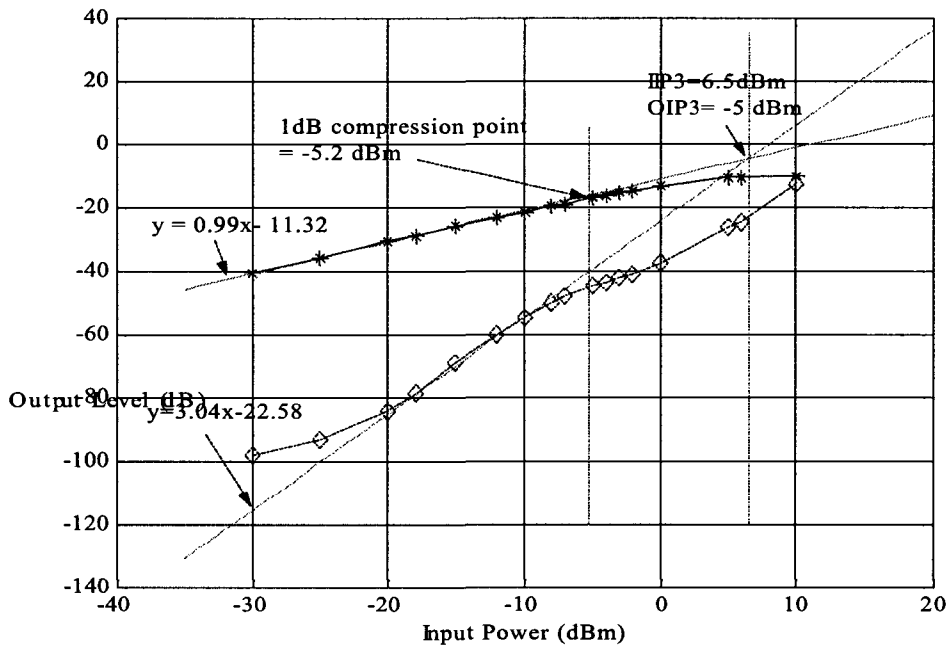

Figure 4.3 1-dB compression point and input third-order intercept point of the switching mixer

For the switching mixer, a $2.45GHz$ $0.45V$ square wave is used as the LO signal. Two RF tones of $2.42GHz$ and $2.43GHz$ are applied at the input of the mixer with equal power levels to perform input third order intercept point analysis. Power levels of both tones are swept from -30dBm to 20dBm to observe the first order and third order nonlinearity behavior, which is shown in Figure 4.3, and its performance is summarized in Table 4.1, and the measured output spectrum of one branch of this passive switching mixer is shown in Figure 4.4.

Table 4.1 Switching mixer performance summary

Process	0.18 μm CMOS
IF frequency	0
LO frequency	$2.45GHz$
LO voltage	$0.6V$
Noise figure(DSB)	$8.8dB$
Conversion gain@-30dBm	-2.2dB
1dB compression point	-5.2dBm
IIP3	6.5dBm
OIP3	-5dBm

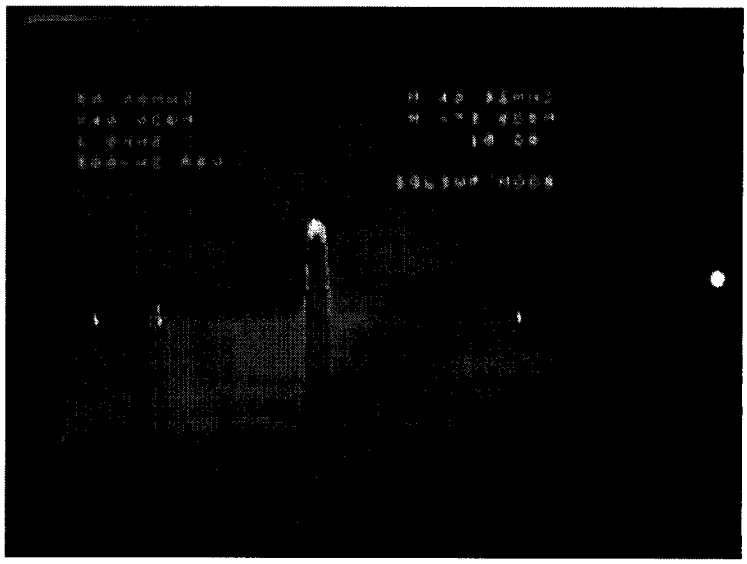

Figure 4.4 Measured output spectrum on one branch of the passive switching mixer

4.3 Active Mixer

As the second element in a direct downconversion receiver, it is desirable that the mixer have high conversion gain and low noise figure. An active mixer topology, based upon the standard Gilbert cell, was selected for this design. The schematic of the mixer core is shown in Fig.4.5. It consists of a driving stage (M1, M2), a switching stage (M3-M6), loads R_L, as well as matching networks and bias circuitry (not shown in Fig.4.5). Driven by a sinusoid LO signal, the mixing operation can be represented as:

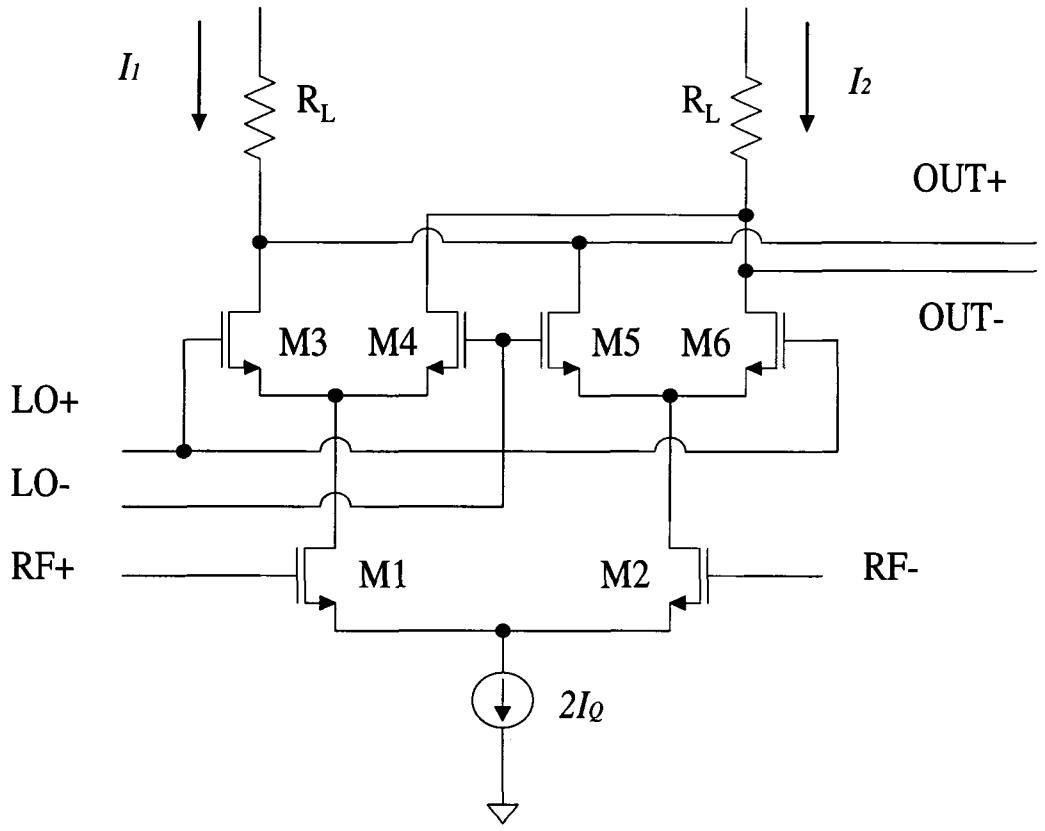

Figure 4.5 Schematic of the Gilbert cell-based mixer core

$$I_{out} = 2g_m V_{RF} V_{LO} \cdot cos2\pi f_{RF} t \cdot cos2\pi f_{LO} t \quad (4.3)$$

$$= g_m V_{RF} V_{LO} \cdot cos2\pi (f_{RF} - f_{LO}) t$$

$$+ g_m V_{RF} V_{LO} \cdot cos2\pi (f_{RF} + f_{LO}) t \quad (4.4)$$

where I_Q is the bias current of the driving stage, g_m is the transconductance of the driving device, V_{LO} is the magnitude of the LO signal, and f_{LO} is the frequency of the LO signal.

From Equation 4.3, it can be observed that double-balanced mixers rejects both the RF and LO frequencies at the output port, as shown in Fig.4.6.

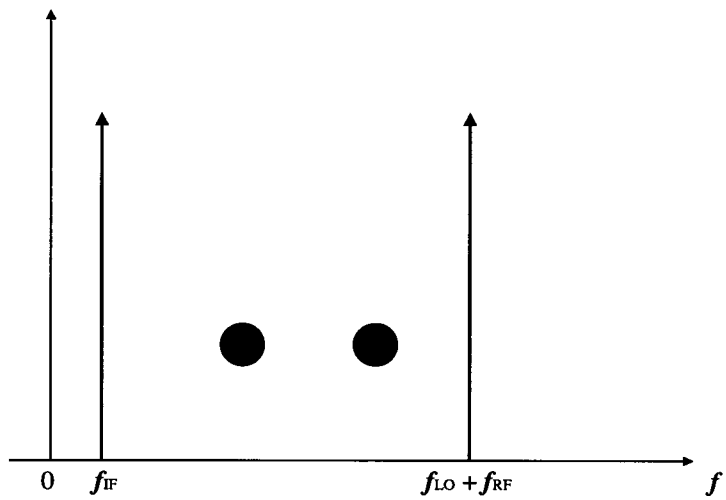

Figure 4.6 Output spectrum of double-balanced downconversion mixers

The conversion gain of this mixer can then be defined as:

$$G_{tran} = \frac{V_{out}}{V_{RF}} = \frac{I_{out} R_L}{V_{RF}} \quad (4.5)$$

$$= g_m V_{LO} R_L \quad (4.6)$$

4.4 Input Matching Network

The function of the input matching network is to match impedance at the RF input port to a certain value, often 50Ω, to achieve low noise performance and high conversion gain. It requires the desired input immittance looking into the matching network that is terminated in the given load immittance to be the conjugate of the source immittance. In order to achieve maximum power transfer, the matching condition requires

$$Z_S = Z_{in}^* \tag{4.7}$$

In order to minimize the noise figure, the optimum source impedance ($Z_{S_{opt}}$) of the driving stage should be matched to the impedance of the source (Z_S), or

$$Z_S = Z_{S_{opt}} \tag{4.8}$$

Simultaneous power and noise matching thus involves satisfying the following condition:

$$Z_{S_{opt}} = Z_{in}^* \tag{4.9}$$

From the above relations, a general strategy for the design of the RF input matching network was developed, as shown in Fig.4.7. Because of the presence of parasitic capacitances at the gates of the driving transistors, an on-chip inductor L_1 is added to the RF port to series resonant the input impedance such that the resulting impedance at desired frequency is purely real. Then a matching section consisting of a series capacitor C_1 and a shunt inductor L_2 can be used to match the remaining resistance to Z_S, which is 50Ω. The series capacitor C_1 would act as a blocking capacitor, and the shunt inductor L_2 would be used as a bias inductor.

The mixing stage also has an important impact on mixer noise performance. Instances of imperfect switching, where both sides of a differential pair are on, will increase the noise figure, and reduce the gain[35]. Therefore, these switching transistors were sized smaller than those of the driving stage.

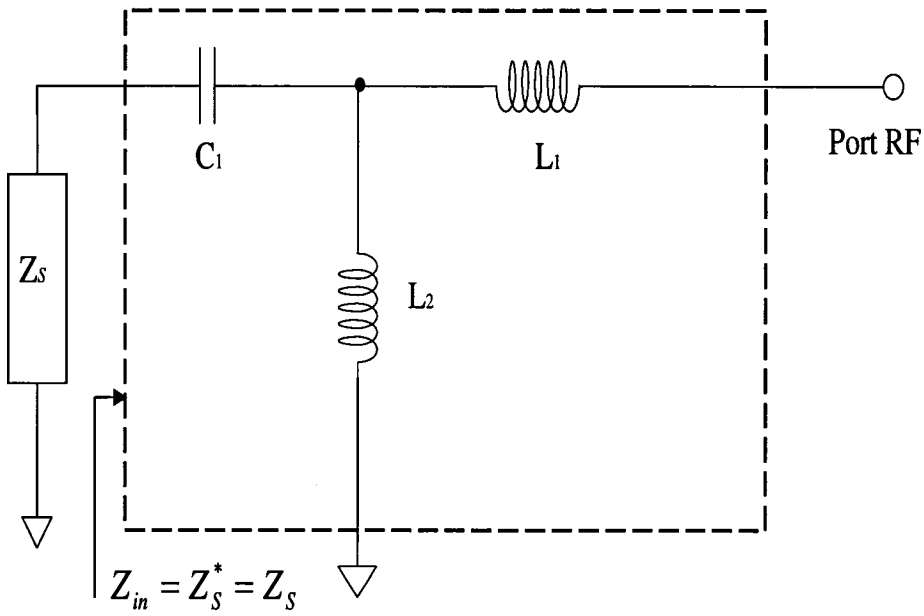

Figure 4.7 The optimum input matching network

In order to facilitate single-ended testing, a baseband output buffer shown in Fig.4.8 is used to take the differential mixer output and to convert it to a single-ended signal. In addition, the buffer provides approximately $4dB$ of gain to the down-converted signal. Its output is matched to 50Ω. The complete schematic of the mixer is shown in Fig.4.9.

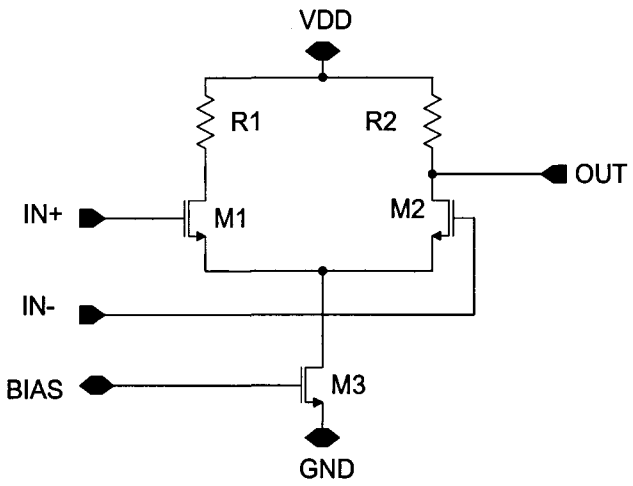

Figure 4.8 VCO output buffer

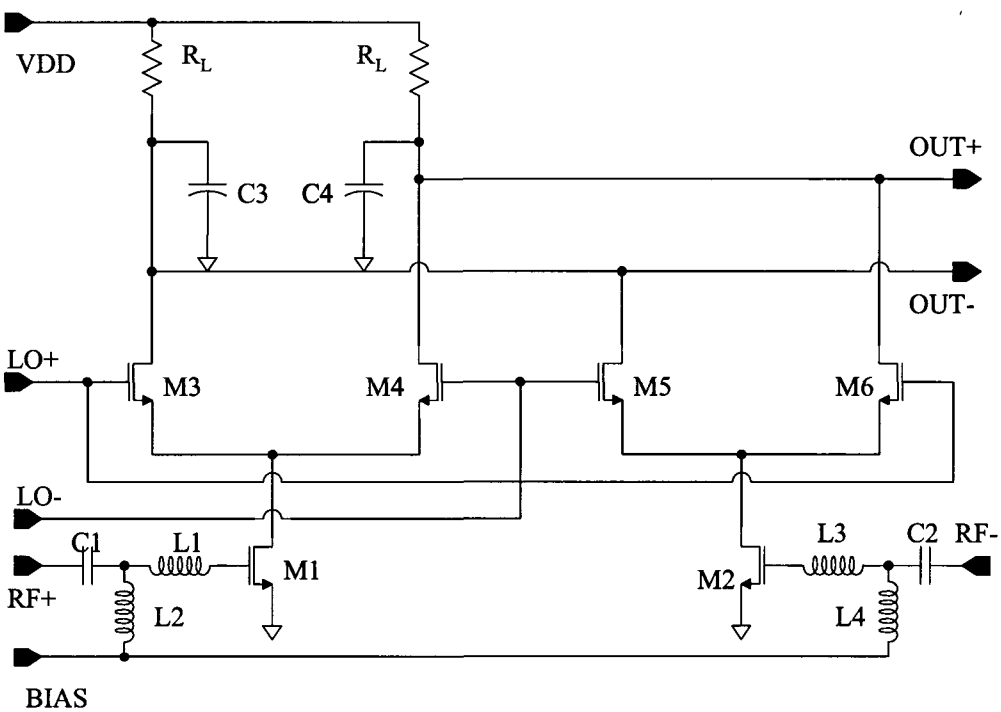

Figure 4.9 Complete schematic of the mixer

4.5 Simulation Results

The double-balanced direct downconversion mixer was designed and simulated in Cadence SpectreRF in $0.18\mu m$ CMOS technology. It is powered with a 1.2V DC supply. The RF signal is $2.41GHz$ at -$30dBm$, and the LO signal is $2.4GHz$ at -$10dBm$.

The simulated double sideband noise figure of the mixer is shown in Fig.4.11. It can be seen that the main contributing noise is the flicker noise $1/f$ noise at the lower frequency range. With increasing frequency, there is only intrinsic thermal noise remaining since the optimum matching network does not contribute noise. In upper band, the flicker noise is mixed up to the LO. Hence, $1/f$ noise becomes the main contributor again due to drop in conversion gain.

In order to investigate the linearity of the mixer, a $2.4GHz$ sinusoid of -$10dBm$ is used as the LO signal. Two RF tones of $2.41GHz$ and $2.42GHz$ are applied at the RF port of the mixer with equal power levels to perform input third order intercept point analysis. Power levels of both tones are swept from -$50dBm$ to $0dBm$ to observe the first order and third order nonlinearity behavior, which are shown in Figs. 4.12 and 4.13.

The mixer consumes $4mW$ from a 1.2V supply, and the output buffer consumes $2.4mW$. Fig. 4.14 shows its layout, and Table 4.2 summarizes the simulated results.

Circuit performance is compared with some previously published RFIC mixers in Table 4.3. This design presents a better performance in noise figure and power dissipation, as well as good linearity. What's most impressive is that this mixer requires only -$10dBm$ LO signal power to drive it, which makes it more suitable for low-voltage and low-power applications.

Table 4.2 Performance summary of the mixer

Process	0.18 μm CMOS
RF frequency	2.41GHz
LO frequency	2.4GHz
LO power level	-10dBm
Supply voltage	1.2V
Bias current	3.4mA
Noise figure(DSB)	9.2dB
Conversion gain@-30dBm	12.25dB
1dB compression point	-16.4dBm
IIP3	-4.5dBm
LO-RF leakage	-31dB

Table 4.3 Performance summary of the mixer

Reference	[52]	[53]	[54]	[55]	This work
Process	$SiGe$	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS
Frequency(GHz)	17.35	5.2	5.8	1.6	2.41
IF(GHz)	0.0	0.1	0.2	0.05	0.01
Conversion Gain(dB)	12.0	20.91	7	-8	12.25
IIP3 (dBm)	-10	-13.6	-2.94	22	-4.5
Noise Figure(dB)	11.5	9.1	14.3	25	9.2
Power Dissipation(mW)	17.8	3.95	6.89	43	4

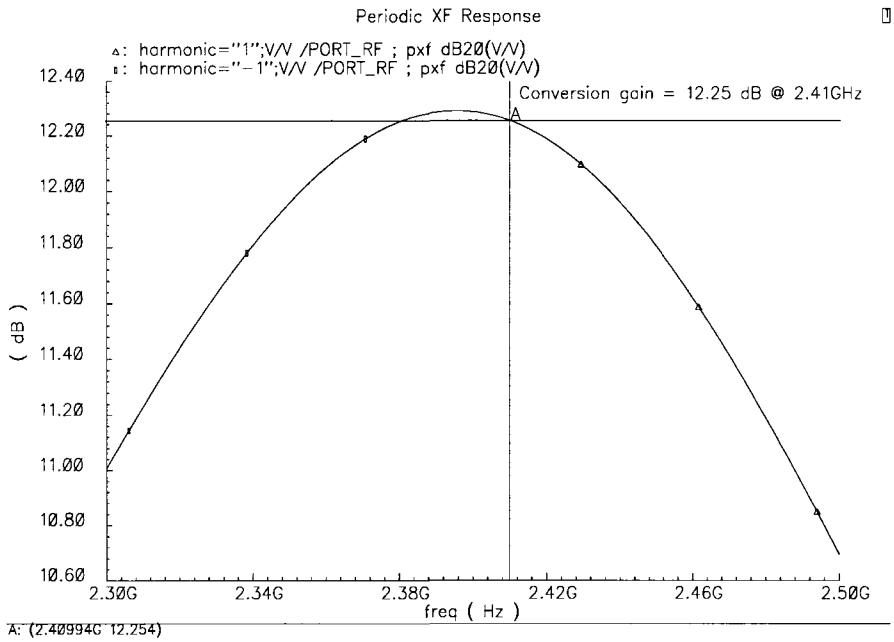

Figure 4.10 Conversion gain of the mixer

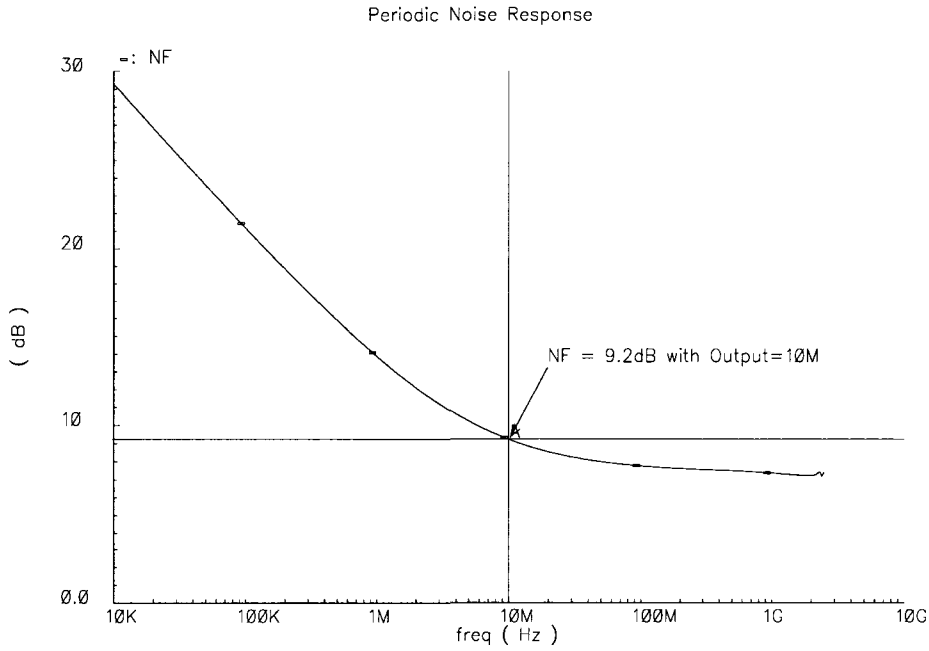

Figure 4.11 Double sideband noise figure of the mixer

4.6 Summary

A double-balanced CMOS direct downconversion mixer based upon a Glibert-cell is presented in this paper. It can work under a low voltage supply of 1.2V, and a low power level LO signal of -10dBm. A simultaneous conjugate input matching network helps to achieve better noise and power performance. With a RF input of 2.41GHz at -30dBm, and a LO signal of 2.4GHz at -10dBm, the conversion gain is 12.25dB, the noise figure is 9.2dB, and the LO-RF leakage is -31dB . It also shows good linearity with its 1dB compression point of -16.4dBm and IIP3 of -4.5dBm.

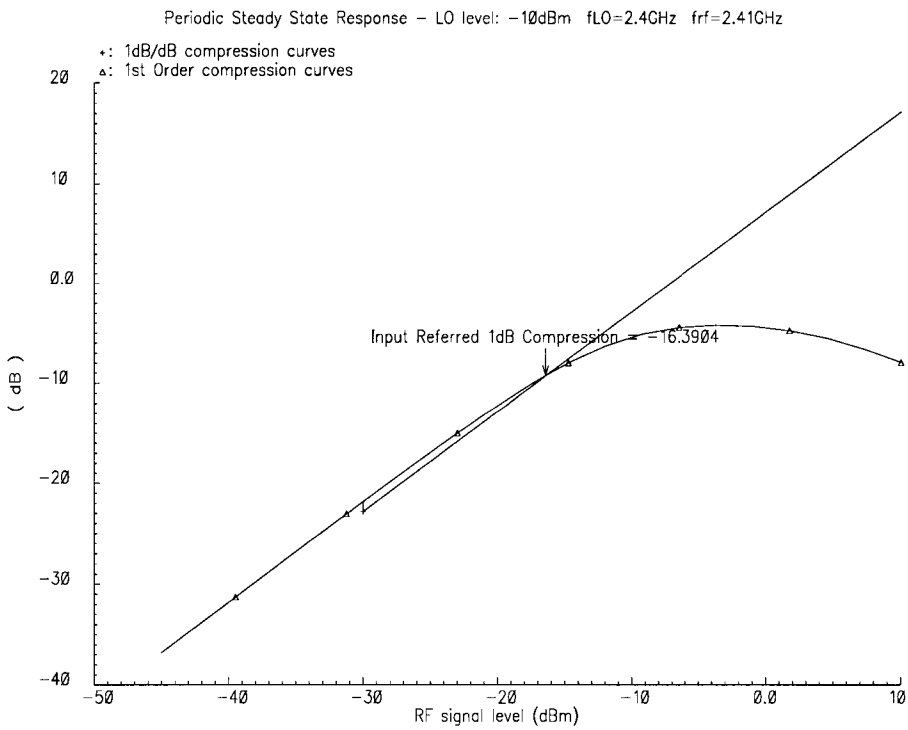

Figure 4.12 1-dB compression point of the mixer

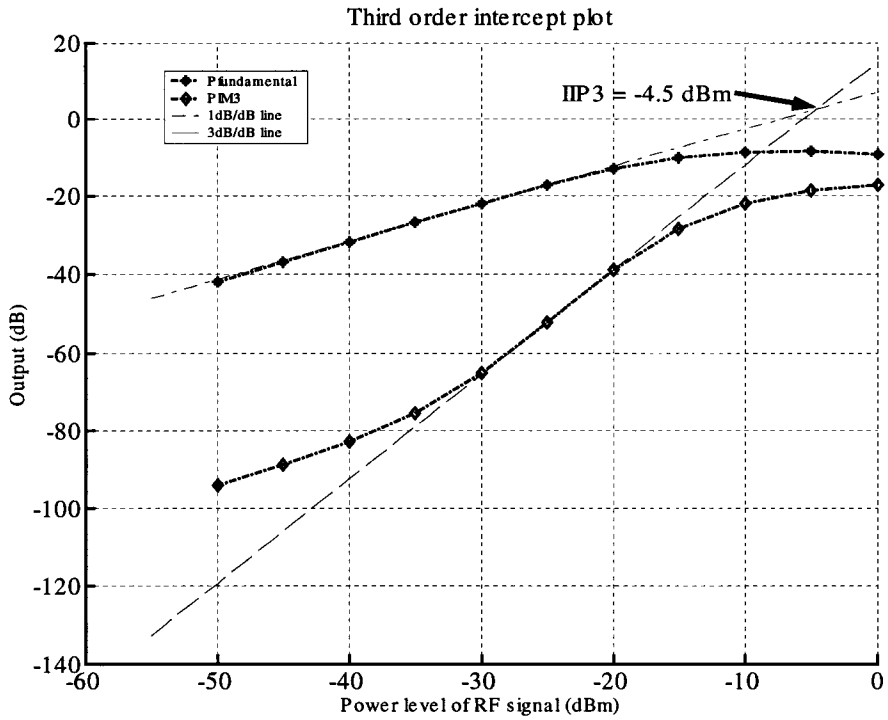

Figure 4.13 Third-order intercept point of the mixer

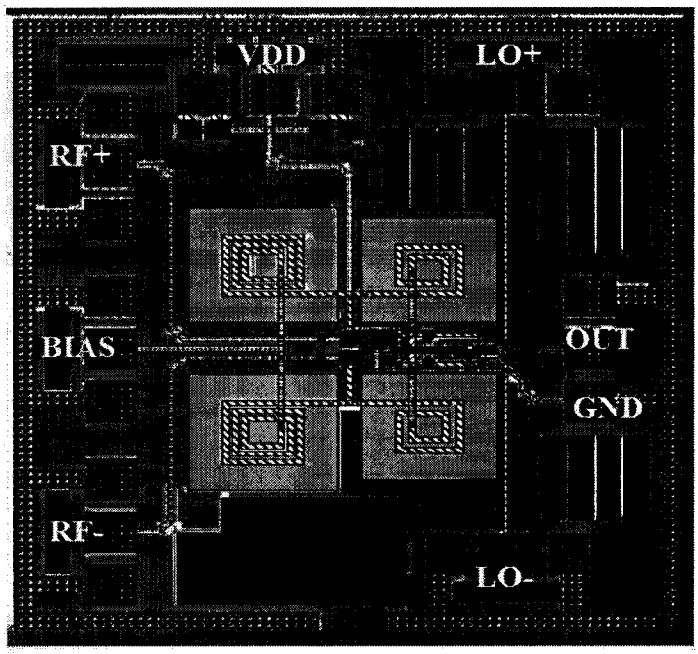

Figure 4.14 Layout of the active double-balanced mixer

CHAPTER 5. DESIGN OF LC VCO

The explosive growth of today's wireless communication market has brought an increasing demand for high performance radio-frequency (RF) circuits in low-cost technologies. Because of advancements in RF CMOS circuits, devices, and passive elements in the last decade, it has become possible to develop a RF system-on-chip (SoC)[2] that integrates RF, analog and digital circuits completely. One major challenge in the design of single-chip transceiver systems is in the design of the voltage-controlled oscillator (VCO) that generates the local oscillator (LO) carrier signal. The phase noise of this VCO is one of the most important parameters for the quality and reliability of data transmission.

For higher quality receivers, a cross-coupled LC oscillator topology has shown better phase noise performance, easier implementation, and differential operation than a relaxation or ring oscillator because the bandpass nature of the resonant tank in the LC oscillator provides the lowest phase noise for a given amount of power dissipation[45]-[48]. A cross-coupled LC oscillator was chosen in this design.

A cross-coupled LC-VCO design is presented in this chapter of this dissertation. It uses on-chip spiral inductors and junction varactors in the resonance LC-tank. To achieve better performance (higher Q) at the target carrier frequency, as well as to get low-power dissipation, a small metal capacitance is included in the tank. The organization of this paper is as follows: Section II talks about low-power low-phase-noise LC VCO basics, Section III describes the design of the proposed VCO, Section IV addresses layout issues, Section V presents simulation results, and Section VI concludes this paper.

5.1 LC VCO Basic

A general LC-VCO can be shown as in Fig.5.1. The inductance L and the capacitance C consist of a parallel resonance tank. R_L and R_C are the parasitic resistances of L and C, respectively. In order to compensate the losses coming from R_L and R_C, active components like CMOS transistors are used to realize a negative resistance $-R$. When the Q-factor is high, the circuit results in a VCO with center frequency

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{5.1}$$

It should be noticed that the capacitance C in (5.1) not only consists of the tunable capacitance of the VCO, but also includes the parasitic capacitances of the inductor, the active components and the load.

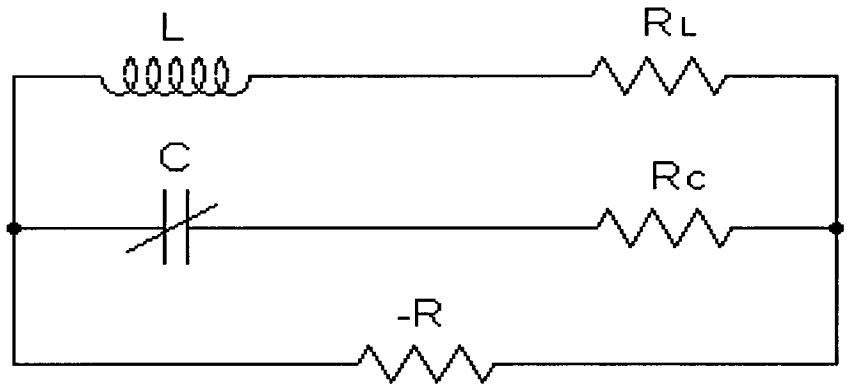

Figure 5.1 Basic LC-VCO

According to [47], the loss in the tank can be expressed as

$$P_{loss} = 4\pi^2 RC^2 f_0{}^2 V_{peak}{}^2 = \frac{R}{4\pi^2 L^2 f_0{}^2} V_{peak}{}^2 \tag{5.2}$$

where R represents the combined losses of the inductance and the capacitance, and V_{peak} is the peak voltage amplitude across the capacitance. It can be observed from (5.2) that

the power loss decreases linearly with the series resistances in the resonance tank, and it also decreases quadratically with the increase of the tank inductance.

A heuristic expression for the phase noise of an LC-VCO was published by Leeson[49] in 1966:

$$S(\Delta f) = F\frac{kT}{{V_{peak}}^2}\frac{R{f_0}^2}{Q^2\Delta f^2} \tag{5.3}$$

where Q is the loaded quality factor of the resonance tank, which is defined as:

$$Q = -\pi f_0 \frac{d\phi}{d(2\pi f)}|_{f=f_0} = \frac{2\pi f_0 L}{R} = \frac{1}{R}\sqrt{\frac{L}{C}} \tag{5.4}$$

and F is the noise factor. Equation (5.3) suggests the most effective way to lower phase noise is to use a tank with higher Q. Tiebout expressed (5.3) further into a more practical expression[47]:

$$S(\Delta f) = F\frac{kT}{{V_{peak}}^2}\frac{R^3}{4\pi^2 L^2\Delta f^2} \tag{5.5}$$

which shows that phase noise is not dependent on f_0 if V_{peak} can be kept constant. It suggests that phase noise can still be optimized in spite of the unavoidable series resistances in a standard CMOS process.

5.2 LC VCO Design

According to the analysis from the previous section, it is clear that an LC-tank with maximal L/R and L/C ratios is needed to achieve low-power consumption and low-phase-noise performance. The schematic of the proposed VCO is shown in Fig.5.2. Two optimized spiral inductors $L1$ and $L2$ are used in series in a differential configuration. Two NMOS transistors $M1$ and $M2$ are coupled in positive feedback to provide a negative resistance. With the inductance value of $2.369nH$, the total capacitance on each node must be $1.856pF$ to provide an oscillation frequency of $2.4GHz$, which includes the inductor's parasitic capacitance, the drain-bulk, gate-drain and gate-source capacitances of the NMOS transistors and the tunable junction capacitance. In order to get low power dissipation, a small fixed metal capacitance is added in the LC-tank. The advantage of doing so is to get smaller die area and smaller power dissipation at the cost of reducing tunable range.

The spiral inductors are implemented using a thick top metal. Its equivalent lumped RLC circuit model is shown in Figure5.3, where L_s is the series inductance, R_s is the metal series resistance, C_s is the overlap capacitance between the spiral and the center tap underpass; C_{ox1} and C_{ox2} are the oxide capacitances between the spiral and the substrate, and R_{sub1} and R_{sub2} are silicon substrate resistances, while C_{sub1} and C_{sub2} are silicon substrate capacitances. The quality factor of a spiral inductor is defined as the ratio of energy stored in it over energy lost in one oscillation cycle[30].Metal wire resistance, capacitive coupling to the substrate, and magnetic coupling to the substrate limit the Q-factors of on-chip spiral inductors.

The junction varactors are implemented using a P+ active area in an N-Well. Its capacitance can be tuned with the control voltage V_{Tune}, which controls the bias voltage of the N-Well. Because the N-Well is a common-mode node, its parasitic capacitance to the substrate is not important. Its equivalent circuit is shown in Fig.5.4, where D is

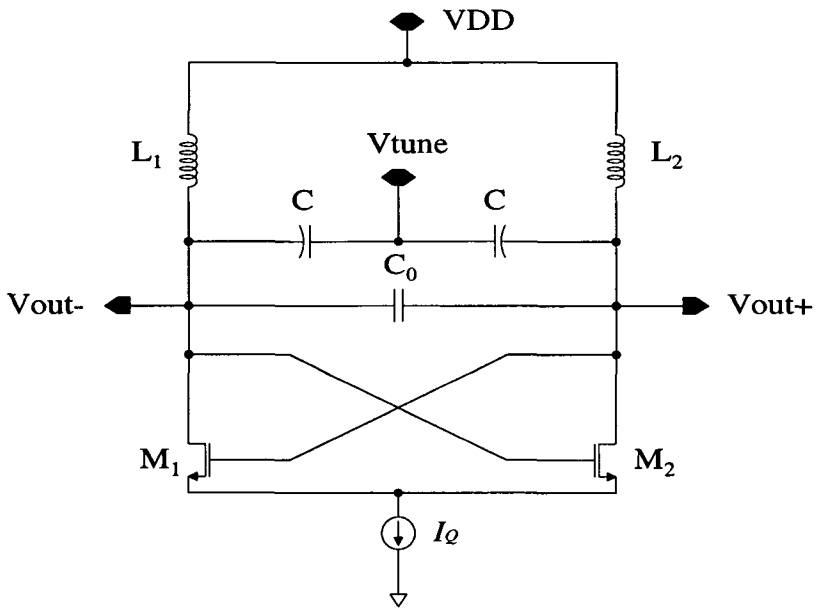

Figure 5.2 Schematic of the VCO

the diode between P+ and N-Well, C_p is the parasitic capacitance, and C_{sub1}, C_{sub2} and R_{sub1} are substrate capacitances and resistance, respectively.

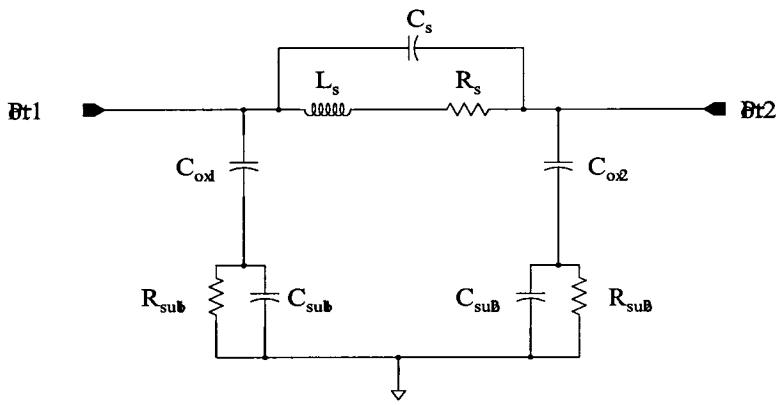

Figure 5.3 Spiral Inductor Model

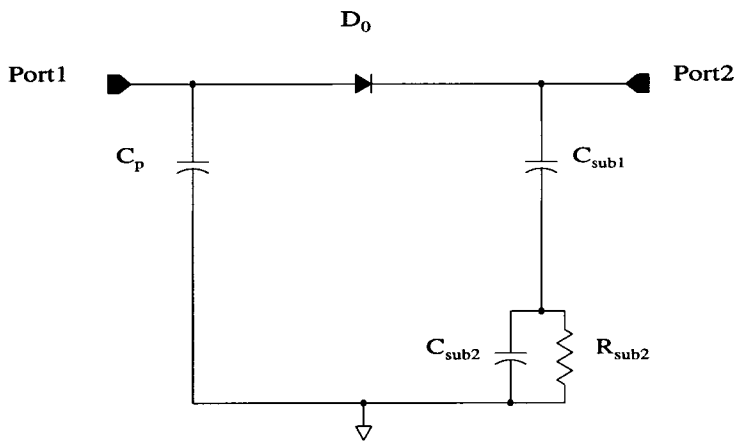

Figure 5.4 P+/NW Junction Varactor Model

5.3 Simulation Results

The layout of the VCO is shown in Fig.5.5, and the transient response of the VCO output is shown in Fig.5.6, while the phase noise performance is shown in Fig.5.7 for a carrier frequency of 2.4 GHz. Phase noise at 100 kHz offset from the carrier is -101.9 dBc/Hz, while the phase noise at 1 MHz offset is -122.1 dBc/Hz, and -131.6 dBc/Hz at 3 MHz. The tuning characteristic of the VCO is shown in Fig.5.8, and its performance is summarized in Table 5.1.

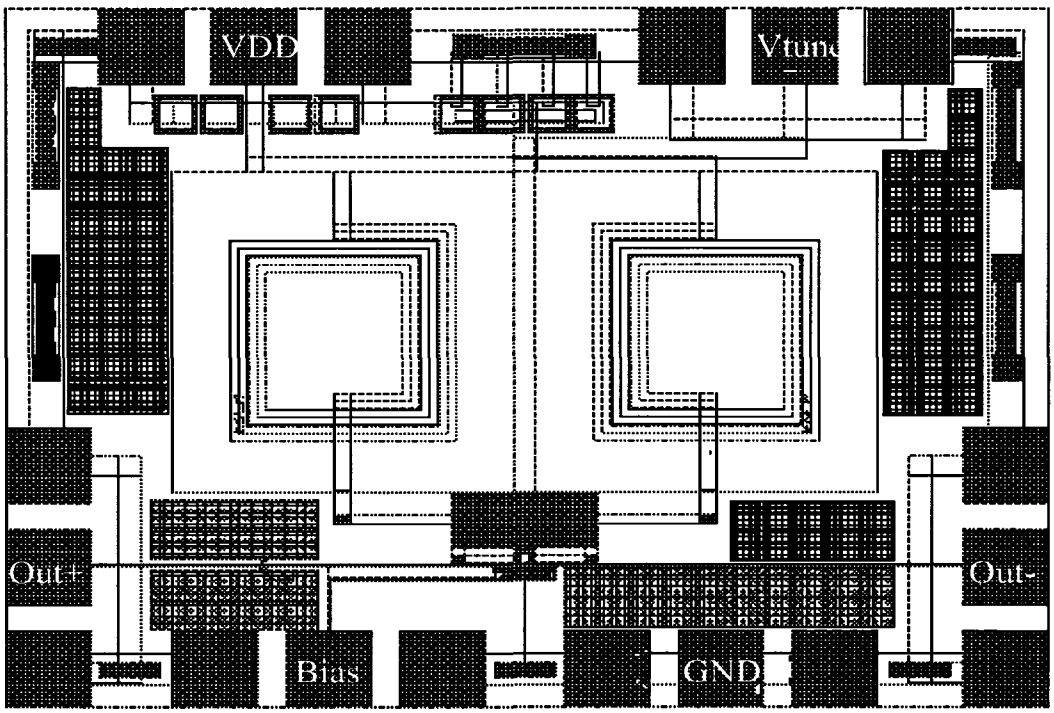

Figure 5.5 Layout of the VCO

In order to make comparisons between different VCOs with respect to power dissipation, carrier frequency and phase noise, three figure of merit (FOM) expressions are used:

$$FOM1 = 20logf_0 - S(\Delta f) - 10logP \tag{5.6}$$

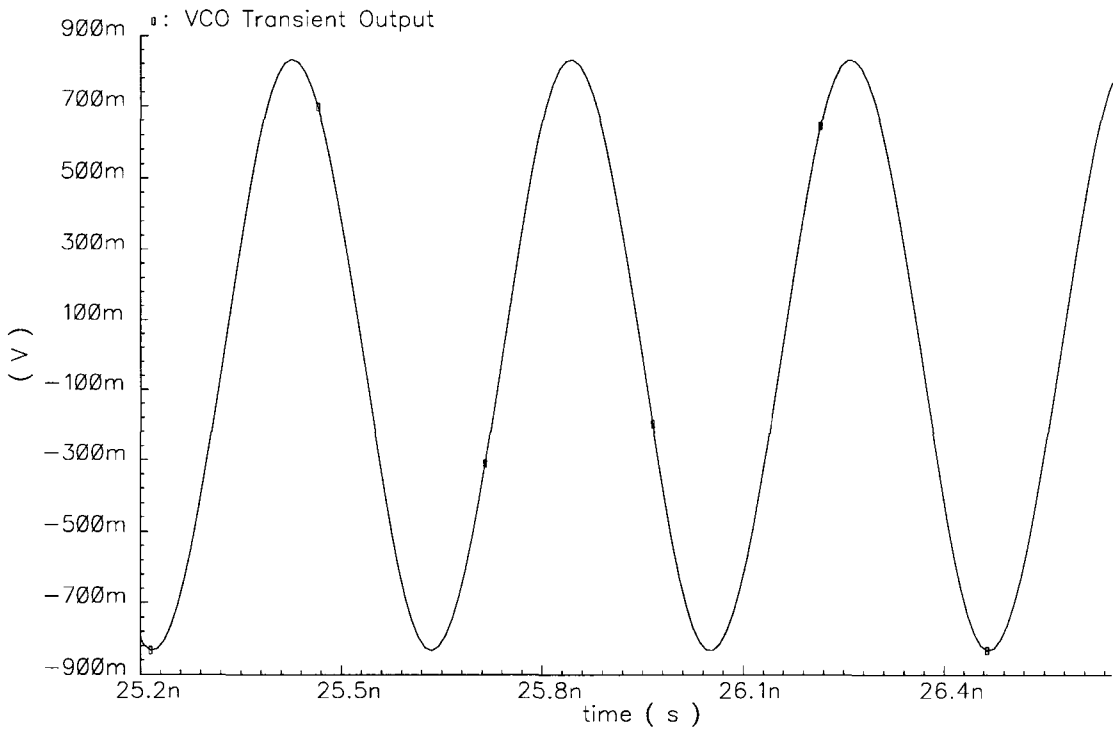

Figure 5.6 Transient Response of the VCO

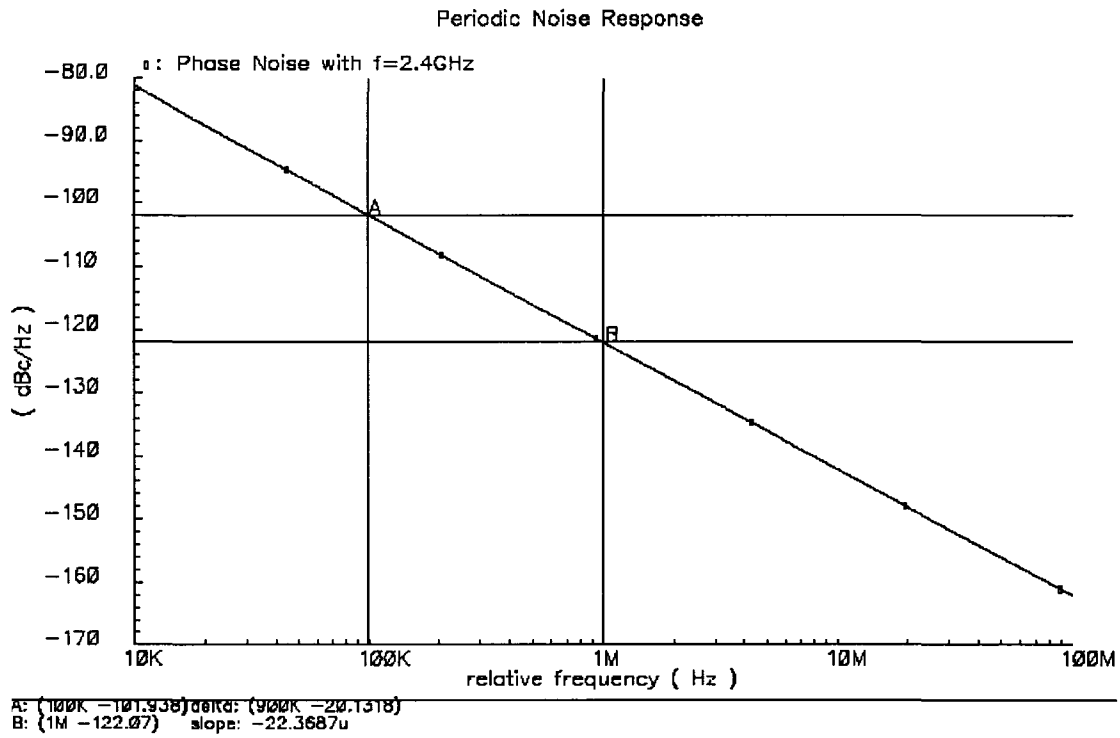

Figure 5.7 Phase Noise of the VCO with $f_0 = 2.4GHz$

for $\Delta f = 100kHz$[51];

$$FOM2 = 10log[\frac{kT}{P}(\frac{f_0}{\Delta f})^2] - S(\Delta f) \tag{5.7}$$

for $\Delta f = 1MHz$[48] and

$$FOM_3 = 20log\frac{\Delta f}{f_0} + S(\Delta f) + 10logP + 30 \tag{5.8}$$

for $\Delta f = 3MHz$[47], where f_0 is the carrier center frequency, Δf is the frequency offset from the center, P is the power consumed by the VCO, and $S(\Delta f)$ is the phase noise at a frequency Δf from f_0. Table 5.2 compares the simulated results of this work with some recently reported fully integrated LC VCOs in standard CMOS process using the three FOM equations. It can be seen this work achieves a good phase noise performance with very low power dissipation through a wide range of offset frequency.

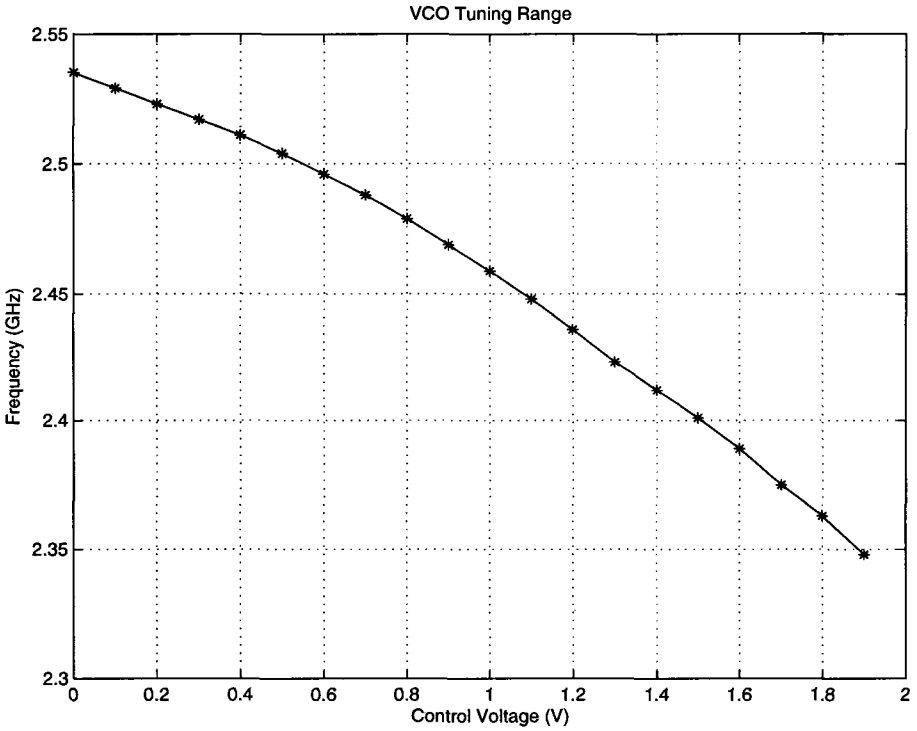

Figure 5.8 Tuning Range of the VCO

Table 5.1 VCO performance summary

Process	0.18 μm CMOS
Supply voltage	1.2 V
Frequency	2.4 GHz
Power dissipation	2.2 mW
Tuning Range	175 MHz
Phase Noise @ 100 kHz	-101.9 dBc/Hz
Phase Noise @ 600 kHz	-117.6 dBc/Hz
Phase Noise @ 1 MHz	-122.1 dBc/Hz
Phase Noise @ 3 MHz	-131.6 dBc/Hz

Table 5.2 VCO Performance Comparison

Reference	f_0 (GHz)	Δf (Hz)	P (mW)	$S(\Delta f)$ dBc/Hz	FOM
[50]	1.4	100 k	3	-107	315
This work	2.4	100 k	2.2	-101.9	316.2
[47]	5.8	1 M	5	-112	6.27
[57]	5.35	1 M	7	-116.5	9.12
[59]	5.8	1 M	2.62	-115	11.64
This work	2.4	1 M	2.2	-122.1	12.1
[46]	1.8	3 M	20	-143	-185.5
[60]	2.5	3 M	2.6	-131	-186.03
This work	2.4	3 M	2.2	-131.6	-186.30

5.4 Summary

A low-power, low-phase-noise design of a fully-integrated 2.4GHz CMOS cross-coupled LC VCO is presented. Junction varactors are used to realize the tunable capacitance. Simulation results have shown excellent phase noise performance as compared with other recently reported CMOS LC VCOs. However, because of the relatively small capacitance of junction varactors, the tuning range of this VCO is only around 7% of the carrier center frequency. It is possible to achieve wider tuning range by using MOS varactors because of their relatively large capacitance.

CHAPTER 6. CONCLUSIONS

6.1 Summary

This work demonstrated the successful analysis, design and simulation of several CMOS RF building blocks that can be used for low-voltage, low-noise direct downconversion receiver for WLAN applications. The need for these building blocks, was shown to stem from the demand for increasing data rates in wireless communications. Early sections of this dissertation discussed direct downconversion techniques and explained the advantages as well limitations of these techniques. The design of a low voltage, low power LNA was demonstrated using a parallel capacitance and an interstage inductance. A theoretical analysis was developed on the effects of both components to show improvement in noise and power performance of the LNA.

In order to achieve direct downconversion, two types of mixers were presented: A passive switching mixer, and an active double-balanced mixer. The passive switching mixer helps to solve the problem of flicker noise, but suffers power loss. While the double-balanced architecture helps to relieve the problems of DC offset and second-order distortion.

At the end of this dissertation, a partially tunable cross-coupled LC VCO was presented. It uses on-chip spiral inductors and junction varactors in the resonance LC-tank. The use of the partially tunable varactor helps to improve phase noise performance, but it also limits the VCO's tuning range.

6.2 Future Work

The use of both a parallel capacitance and an interstage inductance is an important contribution of this work. Further studies need to be done on direct downconversion receivers to overcome the four problems mentioned in Chapter 1. New circuit topologies should be investigated to achieve a reasonably low power dissipation, low noise and better linearity.

More theoretical analysis of the fundamental limitations on the absolute minimum power consumption of a DCR is necessary. It will prove useful to quantify further the trade-offs with power dissipation such as noise figure and dynamic range. Such analysis would provide designers with valuable information necessary to optimize their design for a desired objective.

Another related research area is to use MOS varactors in a cross-coupled LC VCO design. It should provide better phase noise performance than junction varactors, as well as wider tuning range.

BIBLIOGRAPHY

[1] R.H. Caverly, S. Smith, J.G. Hu and R. Nichols, "CMOS RF circuits for integrated wireless systems," in *Digest IEEE MTT-S'1998*, vol.3, pp.1851-1854, June 1998.

[2] A. Matsuzawa, "RF-SoC — expectations and required conditions," *IEEE Trans. Microwave Theory and Techniques*, vol.50, no.1, pp.245-253, Jan.2002.

[3] T. Cho, E. Dukatz, M. Mack, D. Macnally, M. Marringa, S. Mehta, C. Nilson, L. Plouvier and S. Rabii, "A single-chip CMOS direct-conversion transceiver for 900MHz spread-spectrum digital cordless phones," in *Proc. ISSCC'1999*, Feb. 1999.

[4] A. Parssinen, J. Jussila, J. Ryynanen, L. Sumarien and K.A.I. Halonen, "A 2GHz wide-band direct conversion receiver for WCDMA applications," *IEEE J. Solid-State Circuits*, vol.30, no.12, pp.1893-1903, Dec. 1999.

[5] J. J. Kucera, "Wideband BiCMOS VCO for GSM/UMTS direct conversion receivers", in *Proc. ISSCC'2001*, pp.374-375, 466, Feb. 2001.

[6] A.A. Abidi, "Direct-conversion radio transceivers for digital communications", in *Proc. ISSCC'1995*, pp.186-187, 363-364, Feb. 1995.

[7] W. Namgoong and T.H. Meng, "Direct-conversion RF receiver design", *IEEE Trans. Communications*, vol.49, no.3, pp.518-529, Mar. 2001.

[8] Kittel, *Thermal Physics*, pp.98-102, Wiley, New York, 1969.

[9] J.B. Johnson, "Thermal agitation of electricity in conductors," *Phys. Rev.32*, pp.97, 1928.

[10] H. Nyquist, "Thermal agitation of electric charge in conductors," *Phys. Rev.32*, pp.110, 1928.

[11] H.T. Friis, "Noise figure of radio receivers", in *Proc. IRE*, vol.32, pp.419-422, July 1944.

[12] R.J. Weber, *Introduction to Microwave Circuits: Radio Frequency and Design Applications*, Wiley, New York, 2001.

[13] F. Splitter, "Design and analysis of a linear phase-locked loop of wide dynamic range," *IEEE Tran. Comm.*, vol.14, pp.857-857, Dec. 1966.

[14] P. Wambacq and W. Sansen, *Distortion Analysis of Analog Integrated Circuits*, Kluwer, Boston, MA, 1998.

[15] M. Schetzen, *The Volterra and Wiener Theories of Nonlinear Systems*, Wiley, New York, 1980.

[16] B. Razavi, "Design considerations for direct-downconversion receivers", *IEEE Trans. Circuits and Systems*, vol.44, pp.428-435, June 1997.

[17] B. Razavi, "A 5.2GHz CMOS receiver with 62dB image rejection", in *Symp. VLSI Circuits Dig. Tech. Papers*, vol.1, pp.34-37, 2000.

[18] T. Yamaji, H. Tanimato and H. Kokatsu, "An I/Q active balanced harmonic mixer with IM2 cancelers and a 45^0 phase shifter", *IEEE J. Solid-State Circuits*, vol.33, no.12, pp.2240-2246, Dec. 1998.

[19] T. Melly, A.S. Porret, C.C. Enz and M. Kayal, "A 1.3V low-power 430MHz front-end using a standard digital CMOS process", in *Proc. CICC'1998*, pp.503-506, Santa Clara, CA, May 1998.

[20] A.-S. Porret, T. Melly, D.Python, C.C. Enz and E.A. Vittoz, "A 1V 1mW 434MHz FSK receiver fully integrated in a standard digital CMOS process", in *Proc. CICC'2000*, pp.171-174, Orlando, FL, May 2000.

[21] A.-S. Porret, T. Melly, C.C. Enz and E.A. Vittoz, "A low-power low-voltage transceiver architecture suitable for wireless distributed sensors network", in *Proc. ISCAS'2000*, pp.I.56-I.59, Geneva, Switzerland, Apr. 2000.

[22] F.R. Gfeller and U. Bapst, "Wireless in-house data communication via diffuse infrared radiation," in *Proc. IEEE*, pp.1474-1486, Nov. 1979.

[23] K. Pahlavan, T.H. Probert and M.E. Chase, "Trends in local wireless networks," *IEEE Communication Magazine*, pp.88-95, Mar. 1995.

[24] A. Dutta-roy, "Networks for homes", *IEEE Spectrum*, pp.26-33, Dec. 1999.

[25] L. Goldberg, "Wireless LANs: mobile computing's second wave", *Electronic Design*, vol.43, pp.55-72, June 1995.

[26] C. Links, "Universal wireless LANs", *Byte*, vol.19, pp.99-108, May 1994.

[27] H. Ahmadi, A. Krishna and R.O. Lamaire, "Design issues in wireless LANs", *J. High-Speed Networks*, vol.5, no.1, pp.87-104, Jan. 1996.

[28] C. Yue and S. Wong, "Physical modeling of spiral inductors on silicon", *IEEE Trans. Electron Devices*, vol.47, no.3, Mar. 2000.

[29] J.C. Huang, R.-M. Weng, C.-C Chang, H. Kand and K.-Y. Lin, "A 2V 2.4GHz fully integrated CMOS LNA", in*Proc. ISCAS'2001*, vol.4, pp.466-469, May 2001.

[30] T.H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, Ch.11, 1998.

[31] P. Andreani and H. Sjoland, "Noise optimization of an inductively degenerated CMOS low noise amplifier," *IEEE Trans. Circuits Systems II*, vol.48, pp.835-841, Sep. 2001.

[32] B. Razavi, R.H. Yan and K.F. Lee, "Impact of distributed gate resistance on the performance of MOS devices," *IEEE Trans.Circuits Systems I*,vol.41,pp.750-754,Nov. 1994.

[33] D.K. Shaeffor and T.H. Lee , "A 1.5V 1.5GHz CMOS low noise amplifier," *IEEE J.SOlid-State Circuits*, vol.32, no.5, pp.745-759,May 1997.

[34] B. Gilbert, "A precise four quadrant multiplier with subnanosecond response," *IEEE J. Solid-State Circuits*, pp.365-373, Dec. 1968.

[35] A. Rofougaran, J.Y.-C. Chang, M. Rofougaran and A.A. Abidi, "A 1GHz CMOS RF front-end IC for a direct-conversion wireless receiver," *IEEE J.Solid-State Circuits*,vol.31, no.7, pp.880-889, July 1996.

[36] A. Abidi, "Direct-conversion radio transceivers for digital communications," *IEEE J.Solid-State Circuits*,vol.30, pp.1399-1410, Dec. 1995.

[37] J. Long, R.J. Weber, "A 1.5mW, 2GHz CMOS Low Noise Amplifier with 0.75dB Noise Figure", *Wireless Communications, 2002, 14th International Conference on*, vol.1, pp.177-180, Jun. 2002.

[38] J. Long, N. Badr and R.J. Weber, "A Sub-1dB noise figure 2.4GHz CMOS low noise amplifier with interstage inductor", in *Proc. RAWCON'2002*, vol.1, pp.165-168, Aug. 2002.

[39] H.S. Kim, W.S. Kim, X. Li and M. Ismail, "A 2.4GHz CMOS low noise amplifier using an inter-stage matching inductor",*Circuits and Systems, 2000, 42nd Midwest Symposium on*, vol.2, pp.1040-1043, 2000.

[40] A.M. Niknjjad and R.G. Meyer, "Analysis, design and optimization of spiral inductors and transformers for Si RF ICs", *IEEE J. Solid State Circuits*, vol.33, no.10, pp.1470-1481, Oct. 1998.

[41] B. Chi and B. Shi, "A 1.8V 2.4 GHZ CMOS on-chip impedance matching low noise amplifier for WLAN applications Circuits and Systems", *Circuits and Systems, 2003, International Symposium on*, vol.2,pp.188 -191, May 2003.

[42] K. Pahlavan, A. Zahedi and P. Krishnamurthy, "Wideband local access: wireless LAN and wireless ATM", *IEEE Communication Magazine*, pp.34-40, Nov. 1997.

[43] W. Hu, Y. Guo, Z. Qiu and L. Yang, "A 1.2-V 2.4-GHz 0.18μm CMOS low noise amplifier", in *Proc. Communications, Circuits and Systems and West Sino Expositions, 2002, IEEE International Conference on*, vol.1, pp.470 -473, June 2002.

[44] J. Craninckx and M. Steyaert, "A 1.8GHz low-phase-noise CMOS VCO using optimized hollow spiral inductors," *IEEE J. Solid-State Circuits*, vol.32, no.5, pp.736-744, May 1997.

[45] P. Andreani and S. Mattisson, "A 2.4GHz CMOS monolithic VCO based on an MOS varactor," in *Proc. ISCAS'1999*, vol.2, pp.557-560, May 1999.

[46] M. Tiebout, "Low-power low-phase-noise differentially tuned quadrature VCO design in standard CMOS," *IEEE J.Solid-State Circuits*,vol.36, no.7, pp.1018-1024, July 2001.

[47] J. Bhattacharjee, D. Mukheijee, E. Gebara, S. Nuttinck and J. Laskar, "A 5.8GHz fully integrated low power low phase noise CMOS LC VCO for WLAN applications", in *Proc. RFIC'2002*, pp.475-478, Jun. 2002.

[48] D.B. Leeson, "A simple model of feedback oscillator noise spectrum", in *Proc. IEEE*, pp.329-330, Feb. 1966.

[49] A. Hajimiri and T.H. Lee, "Phase noise in CMOS differential LC oscillators," in *VLSI Circuits, Dig. Tech. Papers'1998*, pp.48-51, Jun. 1998.

[50] T.I. Ahrens and T.H. Lee, "A 1.4GHz 3mW CMOS LC low phase noise VCO using tapped bond wire inductances", in *Proc. Low Power Electronics and Design'1998*, pp.16-19, Aug. 1998.

[51] M.W. Lynch, C.D. Holdenried and J.W. Haslett, "A 17-GHz direct down-conversion mixer in a 47-GHz SiGe process", in *Proc. RFIC'2003*, vol.1, pp.461-464, June 2003.

[52] T.Chouchane and M.Sawan,"A 5GHz CMOS RF mixer in 0.18μm CMOS technology", in *Proc. CCECE'2003*, vol.3, pp.1905-1908, May 2003.

[53] X. Wang and R. Weber, "A novel low-voltage low-power 5.8GHz CMOS down-conversion mixer", in *Proc. RAWCON'2003*, vol.1, pp.301-304, Aug. 2003.

[54] D. Jakonis and C. Svensson, "A 1.6GHz downconversion sampling mixer in CMOS", in *Proc. ISCAS'2003*, vol.1, pp.I-725-I-728, May 2003.

[55] A. Hajimiri and T.H. Lee, "A general theory of phase noise in electrical oscillators", *IEEE J.Solid-State Circuits*,vol.33, no.2, pp.179-194, Feb.1998.

[56] H. Jacobsson, B. Hausson, H.Berg and S. Gerorgian, "Very low phase-noise fully-integrated coupled VCOs", in *Proc. RFIC'2002*, pp.467-470, Jun. 2002.

[57] C.-M. Hung, B.A. Floyd, N. Farkand and K.O. Kenneth, "Fully integrated 5.35 GHz CMOS VCOs and prescalars", *IEEE Tran.MTT*, vol.49, pp.17-22, Jan. 2001.

[58] T.-Y. Lin, Y.-Z. Juang, H.-Y. Wang and C.-F. Chiu, "A low power 2.2-2.6GHz CMOS VCO with a symmetrical spiral inductor", in *Proc. ISCAS'2003*, vol.1, pp.641-644, May 2003.

[59] S.-M. Wu, R.-Y. Lin and W.-L. Chen, "A 5.8-GHz high efficient, low power, low phase noise CMOS VCO for IEEE 802.11a", in *Proc. SoC for Real-Time App.'2003*, pp.94-97, June 2003.

[60] R.Dehghani and S.M. Atarodi, "Optimised analytic designed 2.5GHz CMOS VCO", *Elec. Letters*, vol.39, no.16, pp.1160-1162, Aug. 2003.

[61] Y. Ou, N. Barton, R. Fetch, N. Seshan, T. Fiez, U.K. Moon and K. Mayaram, "Phase noise simulation and estimate methods:A comparative study", *IEEE Tran. Circuits and Systems II*, vol.49, no.9, pp.635-638, Sep. 2002.

[62] A. Dec and K. Suyama, "A 1.9GHz micromaclioned-based low-phase-noise CMOS VCO", in *Proc. ISSCC'1999*, pp.80-81, Feb. 1999.

[63] P. Vaananen, M. Metsanvirta and N.T. Tchama, "A 4.3GHz VCO with 2GHz tuning range and low phase noise", *IEEE J. Solid-State Circuits*, vol.36, no.1, pp.142-146, Jan. 2001.

ACKNOWLEDGEMENTS

I would like to take this opportunity to express my thanks to those who helped me with various aspects of conducting research and the writing of this thesis. First and foremost, Dr. Robert J. Weber for his guidance, patience and support throughout this research and the writing of this dissertation. His insights and words of encouragement have often inspired me and renewed my hopes for completing my graduate education. I would also like to thank my committee members for their efforts and contributions to this work: Dr. Eric Bartlett, Dr. Degang Chen, Dr.Julie Dickerson and Dr.Fritz Keinert. I would additionally like to thank Dr. Dickerson for her guidance throughout the initial stages of my graduate career and Dr. Bartlett for his inspirational teaching style.